INTERFACE CIRCUIT DESIGNS FOR EXTREME ENVIRONMENTS USING SIGE BICMOS TECHNOLOGY

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INTERFACE CIRCUIT DESIGNS FOR EXTREME ENVIRONMENTS USING SIGE BICMOS TECHNOLOGY

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Finally, I would like to express my gratitude to the Creator and Sustainer of all things. The Love of Jesus Christ, in taking my sins upon Himself, has freed me to live and exist in such a way that I may bear fruit lasting into eternity. I know that today I live because I have hope through the death and resurrection of Jesus Christ. Soli Deo Gloria!

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

SUMMARY

SiGe BiCMOS technology has many advantageous properties that, when leveraged, enable circuit design for extreme environments. This work will focus on designs targeted for space system avioinics platforms under the NASA ETDP program. The program specifications include operation under temperatures ranging from -180°C to +125°C and with radiation tolerance up to total ionizing dose of 100 krad with built-in single-event latch-up tolerance. To the author's knowledge, this work presents the first design and measurement of a wide temperature range enabled, radiation tolerant as built, RS-485 wireline transceiver in SiGe BiCMOS technology. This work also includes design and testing of a charge amplification channel front-end intended to act as the interface between a piezoelectric sensor and an ADC. An additional feature is the design and testing of a 50 Ohm output buffer utilized for testing of components in a lab setting.

CHAPTER I

INTRODUCTION

1.1 Motivation

A renewed push for space exploration over the last decade has opened up research of extreme environment electronics. NASA has set goals of attaining affordable human and robotic exploration of the solar system with the hope of sending humans to the moon by 2020 as a stepping stone to going to Mars. These aggressive goals require technology and infrastructure to be developed while simultaneously benefiting U.S. scientific, security, and economic interests [20]. This work has been funded by NASA's Radiation Hardened Electronics for Space Environments (RHESE) program and, specifically, the "Silicon-Germanium Integrated Electronics for Extreme Environments" project under the Exploration Technology Development Program (ETDP).

Extreme environment electronic applications span the range of cryogenic and high temperatures with total dose and heavy ion radiation exposure. Within the context of lunar missions, the temperatures range from -180°C during lunar night to +120°C during lunar day over 28 day cycles. Given a 10 year lifetime, 100 krad total ionizing dose is expected [3]. Then, robust operation must be achieved over large temperature swings (300°C !) with tolerance to total ionizing dose (TID) radiation, singe event upset (SEU), and latch-up [19].

In space exploration missions to date, electronics have been confined to shielded "warm boxes," in which temperature could be carefully controlled and radiation exposure mitigated, but this comes at extra overhead in launch weight and degraded reliability. Additionally, confining electronics to a couple of locations fundamentally prevents distributed systems from being realized. However, with the application of

SiGe electronics, one can envision SoC/SiP solutions where the bulky, power-hungry warm boxes could be altogether eliminated. This concept bodes well for distributed sensing, control, and monitoring of complex robotics.

The question then arises why BiCMOS technology shows promise for application to extreme environments. To set the context, traditional Si CMOS technologies are known to engage many advantageous properties of FETs including compact digital logic, versatile analog design practices enabled by the FET technology's inherent length/width scalability, system integration, and low wafer and fabrication costs. With a few mask additions, SiGe HBTs can be integrated into existing CMOS processes while maintaining a cost structure similar to that of the parent CMOS technology. At the same time, the SiGe HBT, when added to CMOS, provides a higher speed device at a given technology node. For example, using 0.5 μm CMOS platform with a peak nFET f_T of around 20 GHz [30], a SiGe HBT can be added with a 50 GHz peak f_T. Given the high-speed capability and the better g_m/I_D performance of the NPN HBT, power reductions may also be possible in comparison to CMOS-only solutions at a given technology node. So, a case can be made that at a given mask size or technology node, SiGe HBTs on a BiCMOS platform provide the backbone necessary to tackle millimeter wave, RADAR, and high-speed analog/mixed-signal designs while providing an added performance per given power advantage [11].

Furthermore, SiGe HBTs have been shown to have robust operation at both low and high temperatures as will be shown in Section 1.3. SiGe HBTs are also inherently tolerant to multi-Mrad total ionizing dose typical of extreme environments, which are discussed in Section 1.4. In the context of extreme environments, SiGe designs have been demonstrated in key analog blocks such as op-amps [15] and voltage references [17, 18]. This work aims to address some possible interfaces between on-chip processors, ADCs, and analog nodes and the world external to the semiconductor chip (i.e.

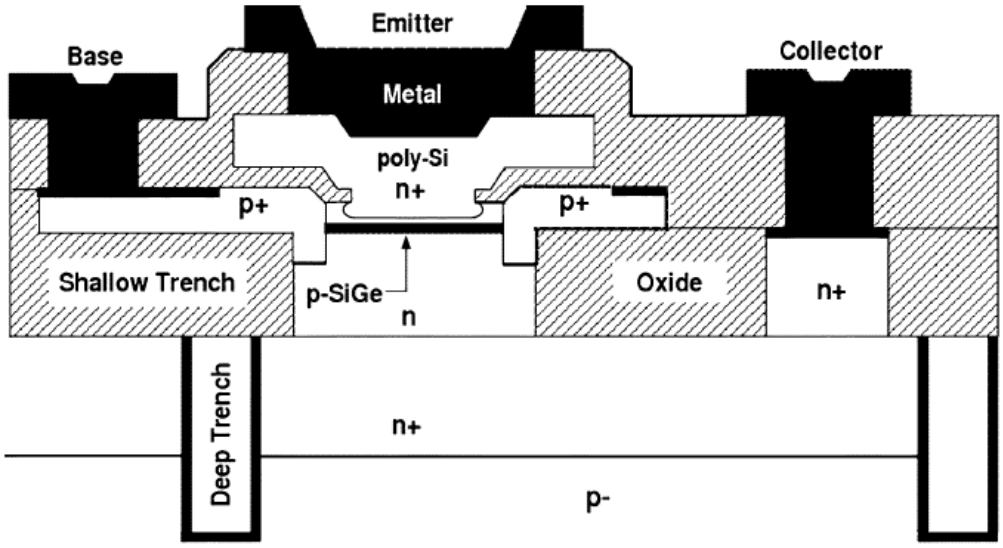

Figure 1: Cross-section of 1st generation 50 GHz SiGe HBT with epitaxial base and pedestal emitter.

communication bus, sensor, external load). Chapter 2 discusses the design and testing of a RS-485 compatible transceiver. Chapter 3 discusses design and testing of a configurable charge amplification and sensing channel for interfacing various sensors. Finally, a low-impedance buffer is discussed in Chapter 4.

1.2 SiGe BiCMOS Technology Overview

The BiCMOS technology used for this work is the IBM SiGe 5AM platform. This technology is built on a P_ substrate including 0.5 μm CMOS and a self-aligned extrinsic base NPN SiGe HBT with a standard graded epitaxial base. A cross-section of a typical 50 GHz SiGe HBT can be seen in Figure 1. Four layers of metallization were used with the top metal being a thick, analog copper enabling on-chip inductor fabrication. Both shallow trench isolation (STI) and deep trench isolation (DT) are employed. Additional notable features include 1.35 fF/μm^2 metal-insulator-metal (MIM) capacitors, low temperature-coefficient polysilicon resistors, high sheet-resistance polysilicon resistors, and Schottky barrier diodes (SBD).

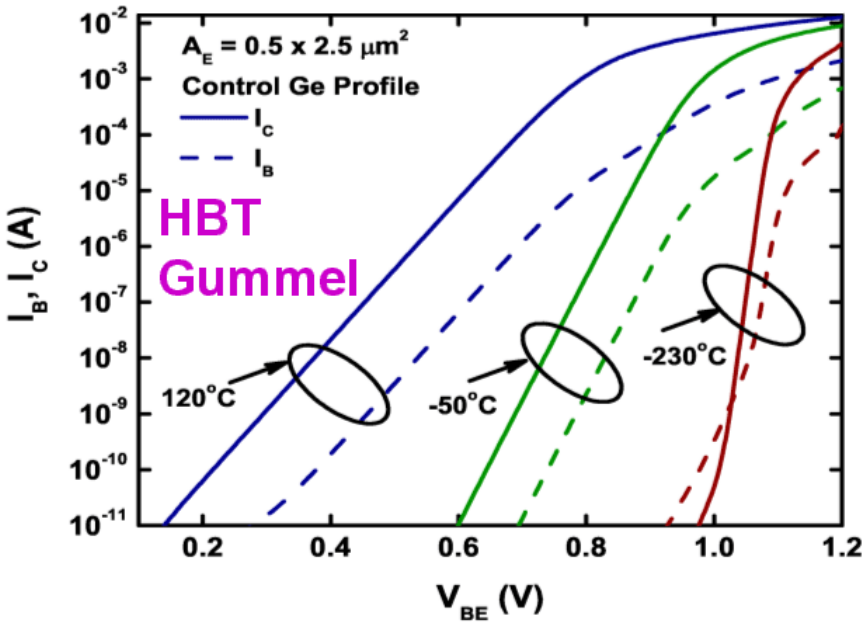

Figure 2: Gummel plot of 0.5 x 2.5 μm^2 SiGe HBT over temperature.

1.3 Performance over Temperature

The HBT used in this work has favorable small-signal performance at low temperatures. In Figure 2, the Gummel plot for a 0.5 μm x 2.5 μm transistor shows the increasing slope of the base and collector currents at low temperatures, demonstrative of improved g_m performance. This does, however, come at the cost of increased headroom since the intrinsic carrier level drops at low temperatures. Therefore, the "on voltage" increases at low temperatures. One may note the base current "foot" in the Gummel plot attributed to tunneling-induced leakage. This leakage limits the minimum current bias-point for useful operation of the HBT in analog circuit applications [4].

Measurements of the peak cutoff frequency, f_T, at temperature points from 393 K down to 4.3 K have shown favorable AC performance at low temperatures. In Figure 3, f_T performance improves at cryogenic temperatures due to beneficial effects of Ge-grading-induced drift field. The improvement, however, is not monotonic as theory would imply [5], but may be a result of minority carrier trapping in the base region

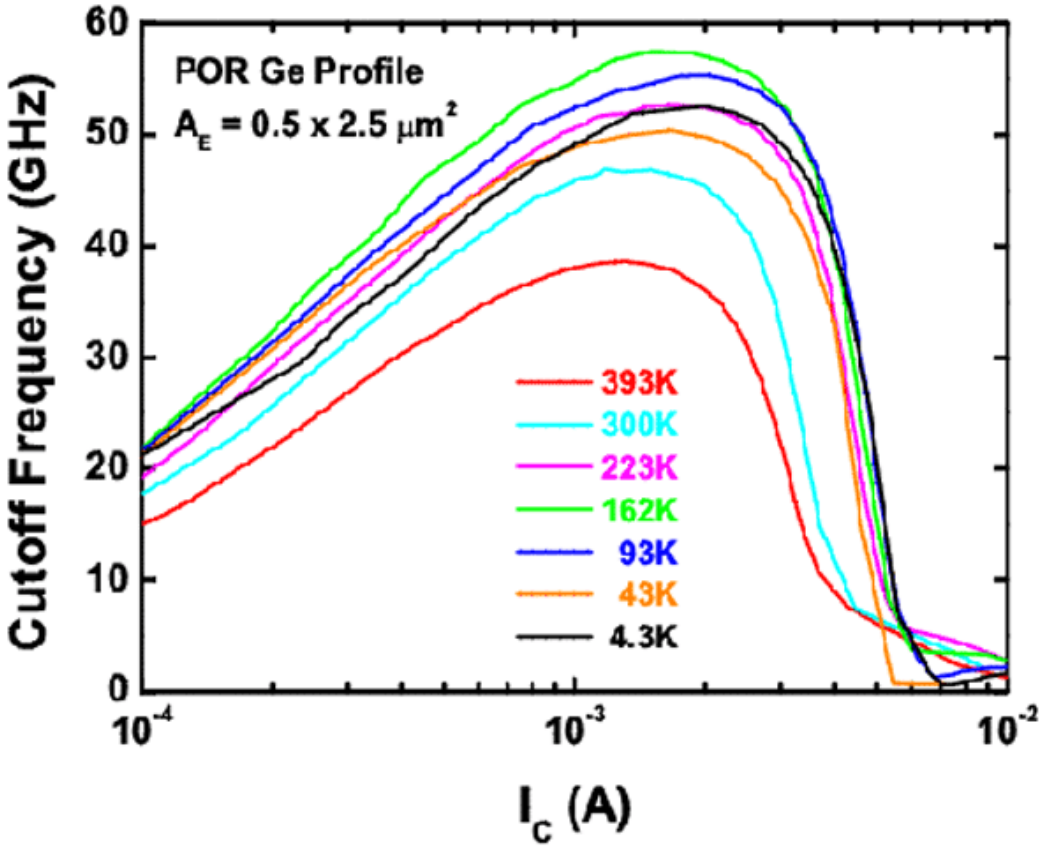

Figure 3: HBT f_T vs. I_c characteristic over temperature.

related to increased base resistance at low temperatures [7]. The best f_T performance was observed at 162 K.

One may of course question the reliability of the SiGe HBTs and the CMOS devices at cryogenic temperatures. For SiGe HBTs, mixed-mode device reliability studies performed to date have shown robust operation under stress at cryogenic as well as high temperatures with no reliability degradation attributed to extreme temperature [6, 33]. CMOS devices are a different story. Hot carrier effects (HCE) are known to adversely impact CMOS reliability. This effect is further accentuated by cryogenic temperatures [10]. Reliability studies extrapolated to 10 years have shown that nFETs at minimum channel length are most susceptible to HCE. Increasing the device length has been shown to significantly reduce observed substrate current linked

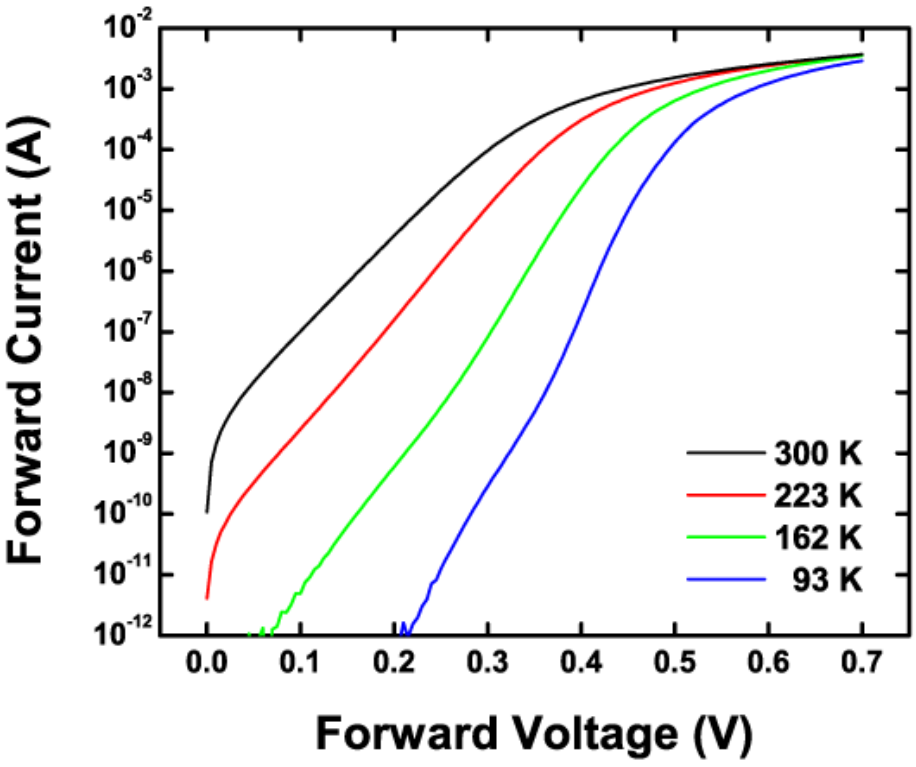

Figure 4: Schottky barrier diode forward mode I-V characteristic.

to HCE and improves the expected lifetime at all temperature points. Increasing the minimum gate length also has the added benefit of reducing radiation induced leakage at the edges of the devices due to shallow-trench oxide interface traps (see Section 1.4). Therefore, a minimum length of 1 μm for the nFETs was imposed. pFETs are inherently less susceptible to HCE, and, therefore, design-kit enforced minimum geometry of 0.5 μm was used.

Schottky barrier diodes were also utilized in designs. The I-V characteristic of a 5 x 5 μm^2 diode is shown in 4. As expected from the dominant thermionic emission transport phenomenon, the I-V slope both gets steeper and has an increased "on" voltage for a given forward current at low temperatures [26].

The lightly-doped polysilicon resistors fabricated over deep-trench isolation provide the highest available sheet resistance within this design process at approximately

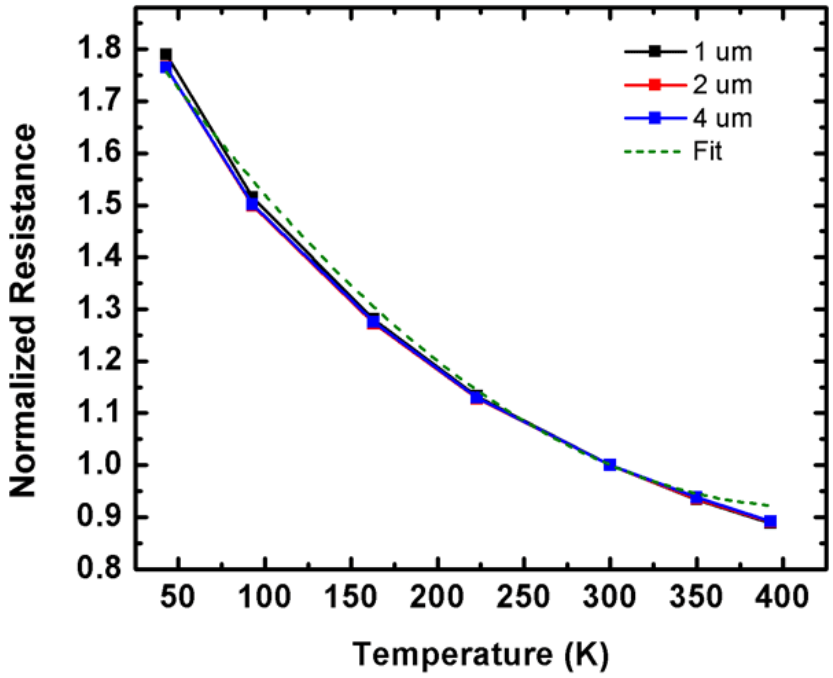

Figure 5: Lightly-doped polysilicon over deep trench resistor temperature profile normalized to 300 K for three widths with 2nd order polynomial fit.

1500 Ω/⊓. Figure 5 shows the performance over temperature of these resistors normalized to 300 K. Three separate data are shown for resistors of 1, 2, and 4 μm width with resistance values of 1 MΩ, 400 kΩ, and 20 kΩ respectively. Note that the temperature profile is not linear but can be approximated by a second-order polynomial characteristic with a negative temperature coefficient. Estimation of the effective resistance at a given temperature is related by

$$R(T) = R_{nominal}\left[\left(6\times10^{-6}\right)(T-300)^2 - \left(1.4\times10^{-3}\right)(T-300) + 1\right], \qquad (1)$$

where T is the temperature in Kelvin and $R_{nominal}$ is the resistance measured at 300 K.

1.4 Performance under Radiation

SiGe HBTs have been tested under gamma rays, x-rays, neutrons, and protons. High energy protons typically have the most substantial effect on device performance [6]. Accumulation of a 1.33 Mrad(Si) total ionizing dose (TID) from a 63 MeV proton

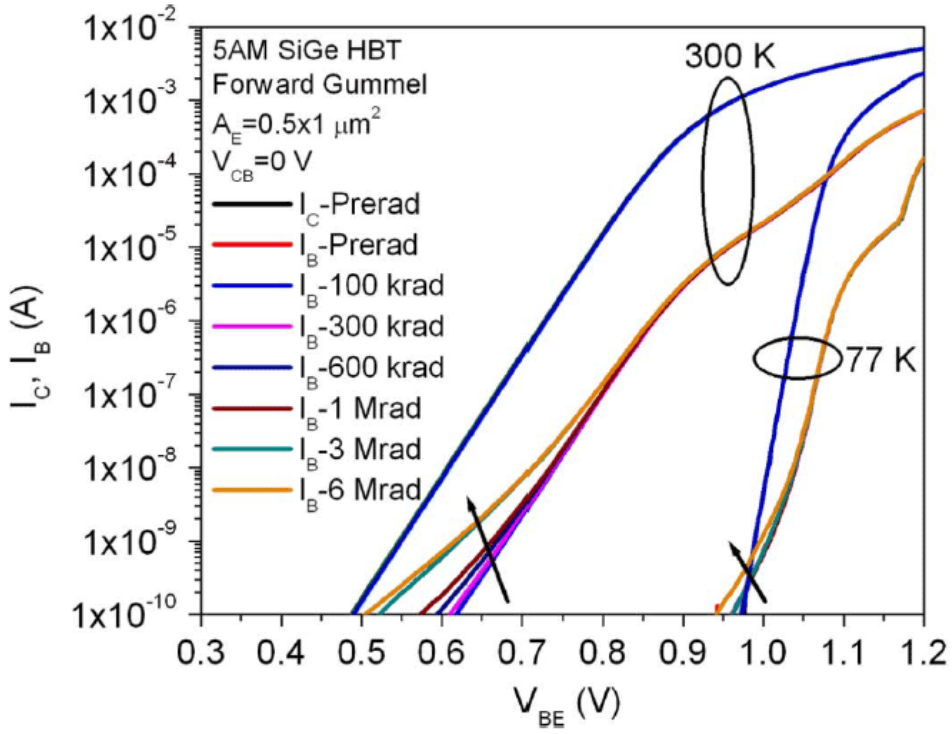

Figure 6: Gummel characteristic of SiGe 5AM HBT measured at 300 K and 77 K under 63 MeV proton radiation beam with up to 6 Mrad total ionizing dose [27].

radiation source (well beyond 100 krad dose needed for targeted applications) produces no significant degradation in peak current gain for circuits biased at collector currents at or above 10 μA. A plot of the radiation response of a SiGe 5AM HBT (Figure 6 [27]) confirms the robustness of the HBT to 100's of krad TID both at 300 K and 77 K. AC performance is similarly unaffected by radiation at these dose levels [5].

CMOS is, however, less tolerant to radiation. Specifically, the shallow-trench isolation along the edges of the nFET channels may trap charge resulting from radiation and, thereby, cause an inversion of the p-type substrate. This in turn creates a drain-to-source leakage path, which can adversely affect performance in off-state devices [2]. Note that this shunt leakage effect is not present in pFET devices. Otherwise, the weak-inversion and strong-inversion states of the nFETs are tolerant to TID up to levels of interest. Ring-type nFET devices have been shown to mitigate the shunt

leakage [12]. These may be applied to future designs as necessary at the cost of some modeling, design, and layout overhead.

As pertaining to circuit design, it is necessary to carefully consider the bias levels of transistors with respect to expected radiation doses. Biasing HBTs at or above 10's of μA ensures that the effects of TID radiation in sensitive analog circuits will be negligible second- or third-order effects. For nFETs and pFETs, again, carefully designing with the current density in mind (taking into account inherent CMOS scalability), one may keep circuit leakage effects to a minimum.

Latch-up due to radiation is also an issue of concern with BiCMOS circuit design. When pFETs and nFETs or HBTs are placed in close proximity, a parasitic transistor can form as a result of the pFET n-well interacting with the adjacent n-type transistors which may cause a high-current latch-up scenario [1]. This parasitic effect may be alleviated with careful layout. Frequent (preferrably continuous) n-well contacts, substrate contacts, and guard bands between opposite type devices reduce these positive feedback paths.

SiGe BiCMOS technology is known to be vulnerable to single-event-upset (SEU) and single-event-transients (SET), but this is also the case with other available CMOS and group III-V technologies. Research is ongoing in this area to understand and improve device and circuit design for SEU and SET tolerance [6].

CHAPTER II

RS-485 COMPATIBLE TRANSCEIVER

2.1 Introduction

Modern robotics systems utilize various analog and digital signals running between sensors, control units, and data-processors. These mixed signal systems may be distributed in various locations throughout the body of the robot. For example, a temperature sensor, ADC, and processor could be located at the nose of a robot while at the tip of an arm a piezoelectric accelerometer with its ADC and processor may be situated. Given the distributed nature of the system, each of the data-processing units and controllers must be able to communicate with other parts of the robot in order to facilitate overall functionality of the robotic system. To accomplish this, a communication bus must be implemented which has sufficient bandwidth and robustness to handle the necessary data traffic.

RS-485, also known as EIA-485, is a standard outlining a serial data communication bus that is widely deployed in industrial and commercial applications. One

Table 1: Transceiver Target Specifications

Parameter	Conditions	Min	Max	Unit
Supply voltage		3	3.6	V
Voltage at any bus terminal	Separately or common mode	-7	12	V
High-level output current		-60		mA
Low-level output current			60	mA
Differential output voltage	$R_L = 54\Omega$	1.5		V
Differential load resistance		54		Ω
Differential load capacitance			50	pF
Rise/fall time	$R_L = 54\Omega$, C_L=100pF		10	ns
Propagation delay	$R_L = 54\Omega$, C_L=100pF		20	ns

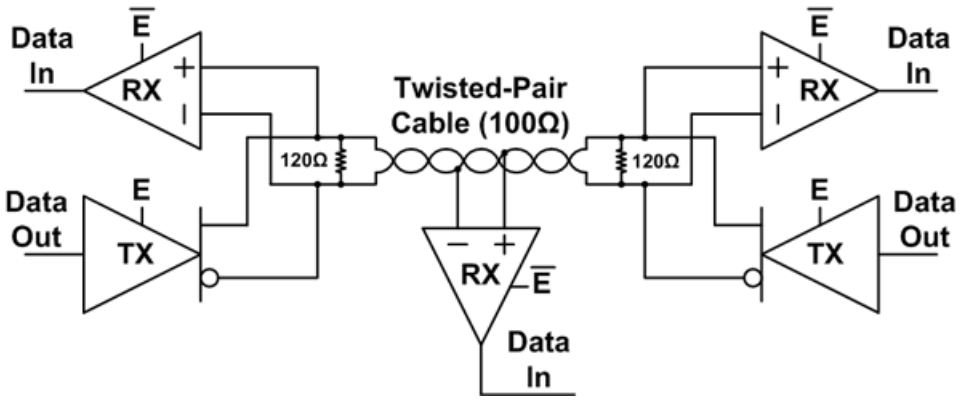

Figure 7: Typical example of RS-485 bus with multiple drivers and receiver with resistive terminations.

formerly popular use was in SCSI-2 and SCSI-3 systems. RS-485 uses digital differential signals to communicate data over distances of up to 1 km [reference]. This technology is known for its noise immunity, bi-directional communication capability (half-duplex), moderate data rates (up to 35 Mbps), designed-in fault tolerance, and general robustness [31] [21]. Figure 7 shows a typical of RS-485 where multiple drivers and receivers coexist and can communicate together in half-duplex mode.

For the NASA extreme environment application, a bandwidth of 10 Mbps was desired. The system into which the transceiver will be integrated operates from a 3.3 V rail, and the design therefore needs to be able to operate with such supplies. It is desirable for the transceiver to have tri-state operation, which is implemented by logical enable controls for the transmitter and receiver. When disabled, the "off" state should be a low-power state. Target electrical and timing characteristics for the

Table 2: Receiver Target Specifications

Parameter	Conditions	Min	Max	Unit
Supply voltage		3	3.6	V
Voltage at any bus terminal	Separately or common mode	-7	12	V
Output load capacitance			15	pF
Rise/fall time	C_L = 15 pF		5	ns
Propagation delay	C_L = 15 pF		55	ns

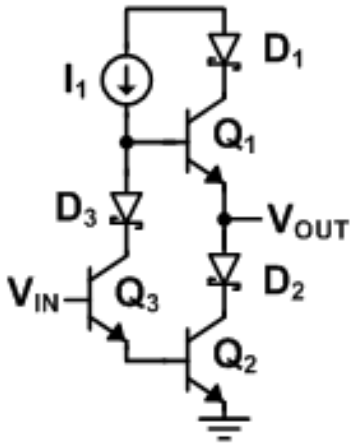

Figure 8: Example commercial transmitter output driver topology.

design were taken from commercial-off-the-shelf parts with similar data rates [23], [29]. Table 1 lists the key target specifications for the transmitter and Table 2 for the receiver. Work on the transmitter and receiver has been presented in [8] in an abbreviated form.

2.2 Design Methodology

Design was performed using Cadence. Compact models were available from IBM for military spec ranges from -55°C to +125°C. However, to reach into the cryogenic temperature range, custom compact models were necessary. These were created through collaboration in the greater NASA Exploration Technology Development Program through which this work was funded. Two additional models were used which modeled the lowest extreme ranging from -180°C to -111°C and then from -111°C to -55°C. Simulations were initially performed using the given IBM models. Further simulations were then performed stretching down to the cryogenic temperature range.

2.3 Transmitter Topology and Design

The transmitter design had a few major constraints in its design. First, the output needs to be able to drive a 3 V differential signal with a differential load of approximately 54 Ω. The value of 54 Ω comes from the parallel combination of two 120 Ω resistive terminations and the load from the input impedance of 16 receivers at 12 kΩ each. Second, the output needs to be robust to voltage transients. This made the use of HBTs desirable due to their superior breakdown performance and the inherent robustness of the diode junctions within the devices. Also, the driver needed to provide sufficiently fast rise and fall times to transmit at 10 Mbps. These requirements are summarized in Table 1.

Initially, commercial literature was examined to see if information on topologies could be located for either bipolar or BiCMOS designs. [22] shows a topology of the form seen in Figure 8. This topology uses an input bipolar device, Q3, to split the signal between devices Q1 & Q2. The pull-up drive capability in this configuration is limited by the value of I1 through the base of Q1. This topology does not necessarily utilize any CMOS devices.

A literature search revealed a handful of BiCMOS inverter topologies in [24] that could be adapted for use at the transmitter's output. One such BiCMOS inverter topology was chosen as seen in Figure 9. This topology is used with a 3.3 V supply and ground in this application. Additional diodes, D1 and D2 were added in order to prevent reverse-biasing of the collector-substrate junctions if differences in the ground potential were present between transmitters on a common bus. This is due to the desired common-mode range of -7 to +12 V as cited in Table 1. An additional change was made to the pre-existing inverter topologies in that the drain of transistor M3 is connected to VDD instead of the output. This enables the output voltage to be slightly lower than in the opposing case due to increased drive capability of M3. Since M3 is connected to the positive rail, the drain to source voltage is larger than in its

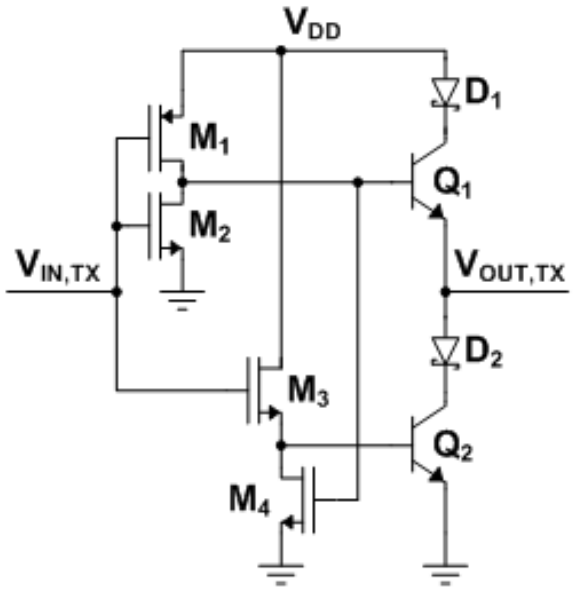

Figure 9: Employed transmitter output driver topology.

original form enabling more current to flow into the base of Q2 for better pull-down capability.

The output driver consists of two of the BiCMOS inverters in parallel paths. The output line driver is intended to interface standard 3.3 V CMOS logic circuits. Therefore, the input to the driver contains a fanout path of 3 CMOS inverters on the non-inverting path prior to the BiCMOS transmit inverter. The inverting path adds one additional CMOS inverter for a total of 3. The idea behind the fanout path was to minimize loading to whatever processor or FPGA interfaces the transmitter, thereby increasing flexibility of the circuit. Additionally, one FET transmission gate was added to the fanout path to allow the output to be disabled. When the output goes into disable mode, FET transistors are appropriately designed to turn-off the output transistors to create a high-impedance "off" or "sleep" state necessary for power-down and half-duplex communications.

One limitation of the transmitter topology is its output swing. When the output is driven high, the maximum output voltage is limited to

$$V_{OUT(max)} = V_{DD} - V_{SD,M1} - V_{BE,Q1}. \quad (2)$$

This output voltage limitation poses a problem especially at low temperatures since diffusion transport in HBTs is thermally activated [5]. Referring back to Figure 4, it is clear that the diode drop seen in Schottky diodes D1 and D2 increases for a given current as temperature decreases. The base-emitter voltage drop of Q1 also increases as temperatures drop (Figure 2). However, the source-drain voltage of M1 should only vary minimally though having some proportionality to temperature.

For the case when the output is being driven low, the minimum voltage is determined by

$$V_{OUT(min)} = V_{CE,Q2} + V_{D2}. \quad (3)$$

Again, the diode drop grows as temperature drops. Also, triode-region operation of the HBT occurs at a higher potential as temperature drops due to the saturation voltage increasing. Using HBTs at the output clearly constrains the low-temperature swing of the transmitter.

To help mitigate this effect, the HBTs and diodes were made large. An array of 32 parallel 0.5 x 2.5 μm^2 HBTs are represented by Q1 and Q2 respectively. Diodes D1 and D2 are arrays of 32 5 x 5 μm^2 Schottky diodes. The current that the HBT array should typically handle is determined by 3 V across a 54 Ω load which equates to 56 mA. Equally dividing the current between 32 HBTs places the current at 1.74 mA per device. Peak f_T occurs between 1 and 2 mA/μm^2 (Figure 3). The individual HBTs should see a current density slightly below peak f_T of about 1.4 mA/μm^2. This should place the HBTs at or near their optimum speed when switching currents.

Figure 10 shows simulation characteristics of the transmitter with a 120 Ω load in parallel with 50 pF. Initially, it was thought that a 120 Ω load would be sufficient

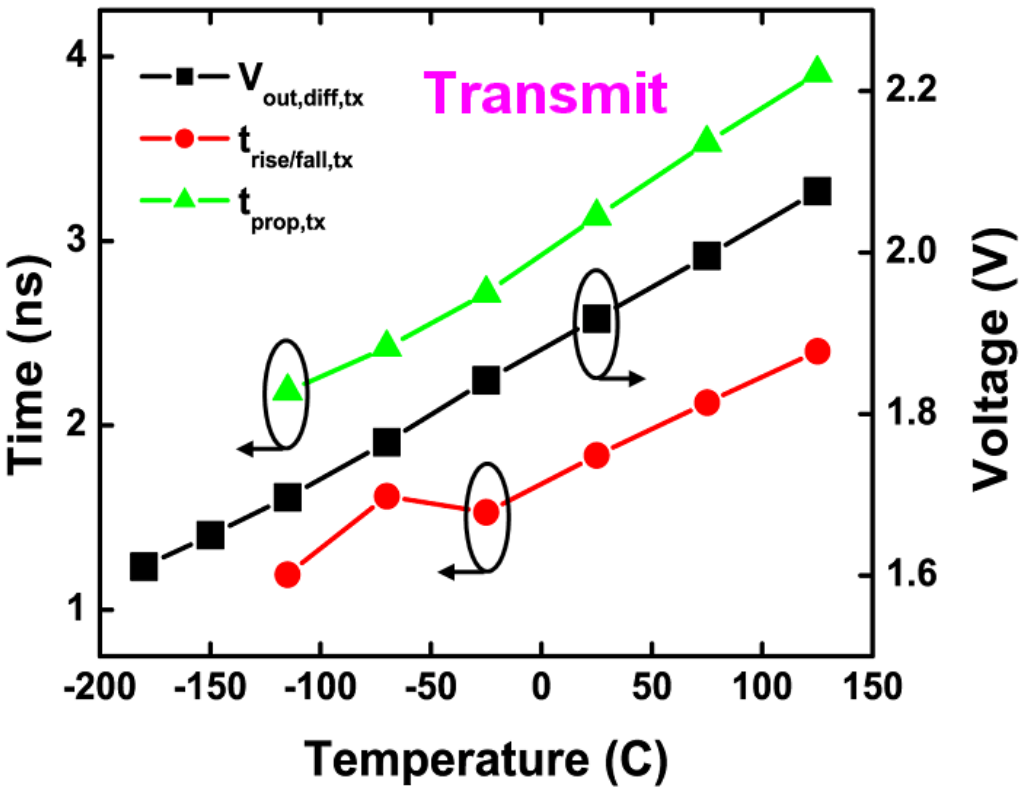

Figure 10: Simulation results with rise/fall times, propagation delay, and differential output voltage over temperature with 50 pF, 120 Ω load.

for operation, but this represents only a single termination resistor. All three plotted characteristics clearly have have proportionality to temperature in simulation. The improved speed of the devices can be attributed to the increase in f_T at low temperatures as seen in Figure 3.

2.4 Transmitter Layout

The layout for the transmitter focused on the HBT array. Due to large currents through the HBTs, self-heating effects could cause an uneven current balance between the 32 parallel devices. This would be an undesirable effect and could lead to an over-current effect if one HBT handled the majority of the current. So, careful attention was placed on symmetry in the device layout to evenly distribute the current as seen in Figure 11. This, however, came at the expense of compactness and metal-routing

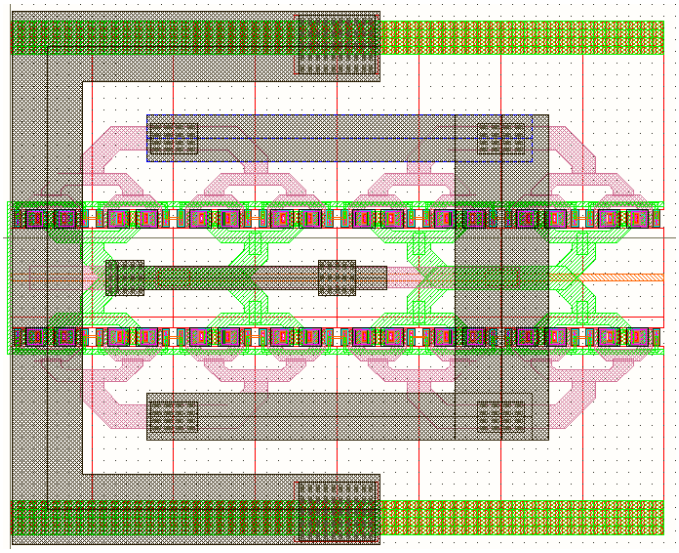

Figure 11: Transmitter HBT array (32 x 0.5 μm x 2.5 μm) with symmetric layout

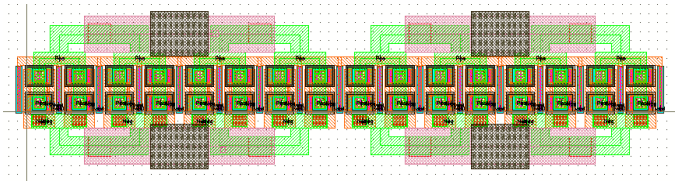

Figure 12: Transmitter Schottky diode array (32 x 5 μm x 5 μm) with symmetric layout

layers used: routing was run on all four metal layers. This is disadvantageous for integration into more complicated systems for which the transmitter was intended. Further revisions of the layout will be necessary to make a more integrable circuit. Figure 12 shows the Schottky diode stack which is also organized symmetrically.

Layout of a full transmitter wired out to pads is found in Figure 13. The pad frame was formed such that the transmitter could be tested at the wafer level with 150 μm pitch probes on an AC probe station. The input would come in through a GSG probe and the differential output would go through a set of GSGSG probes. Pads adapted for a 5-pin DC wedge can be seen on the west side of the layout supplying a positive rail, ground, substrate, and enable signals. Power supply rails were kept separate for the output HBTs and the rest of the circuit in order to allow monitoring of current specifically in the output. The layout shown uses ESD pads which clamp the output

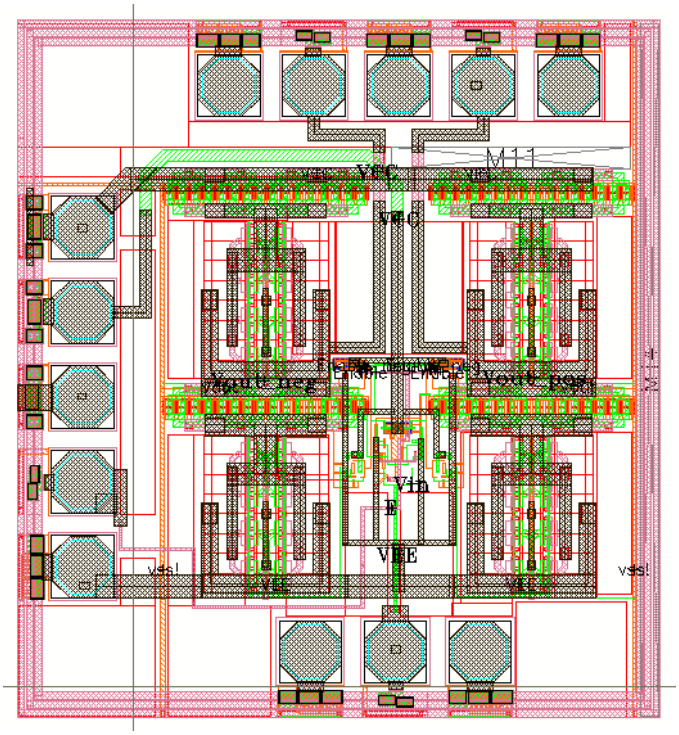

Figure 13: Transmitter layout with 150 μm pitch pad frame.

to a diode drop below ground or a diode drop above the positive supply. However, an additional layout which omitted the ESD pads on the output was taped out in order to allow testing of signals above or below the power rails. A die photo of the completed transmitter is found in Figure 14.

2.5 Receiver Topology and Design

A receiver for an RS-485 system needs to be able to sense the voltage difference between two opposing wires, which represents binary data. The difference is then converted to a single-ended binary signal typical of CMOS logic (3.3 V in this case). This can be achieved with a generic comparator. Additionally, signals are typically noisy, so hysteresis is necessary to prevent unnecessary switching at the transition between states. The OTA comparator topology seen in Figure 15 achieves the function of a comparator with hysteresis.

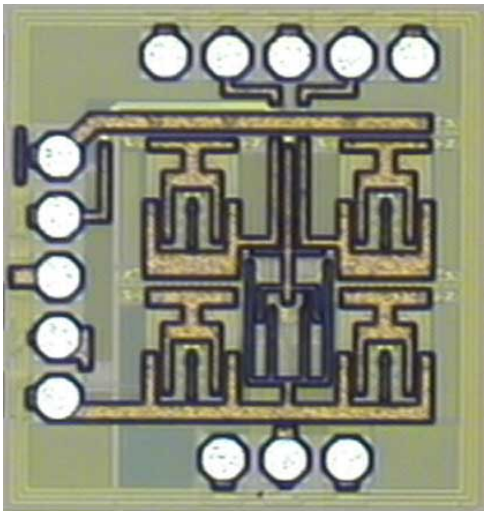

Figure 14: Transmitter die photo

Two source of feedback are present in this topology. Negative current-series feedback happens through the emitters of $Q1$ and $Q2$. Voltage-shunt positive feedback is given through drains of pFET $M2$ and $M3$. So, hysteresis occurs when positive feedback overcomes negative feedback: when $(W/L)_{M2,M3}$ is larger than $(W/L)_{M1,M4}$. For a positive rising edge, initially V_{IN-} has a higher value than V_{IN+}. As V_{IN+} approaches the value of V_{IN-}, the current through $Q1$ is expected to increase up until the point where a current commutation occurs. The comparator switches when collector current equals the sourced current through $Q1$ & $M3$ or $Q2$ & $M2$ [1]. At this point, the currents can be related by

$$i_{Q2} = i_{M4},\ and \tag{4}$$

$$i_{Q1} = i_{M3}. \tag{5}$$

However, noting the relationship between $M3$ and $M4$ followed by a substitution via (4), we find

$$i_{Q1} = i_{M4}\left(\frac{(W/L)_{M3}}{(W/L)_{M4}}\right) = i_{Q2}\left(\frac{(W/L)_{M3}}{(W/L)_{M4}}\right). \tag{6}$$

The current through the HBT can be approximated by

$$i_{c,Q1} = I_s \exp(\frac{V_{be,Q1}}{U_T}), \tag{7}$$

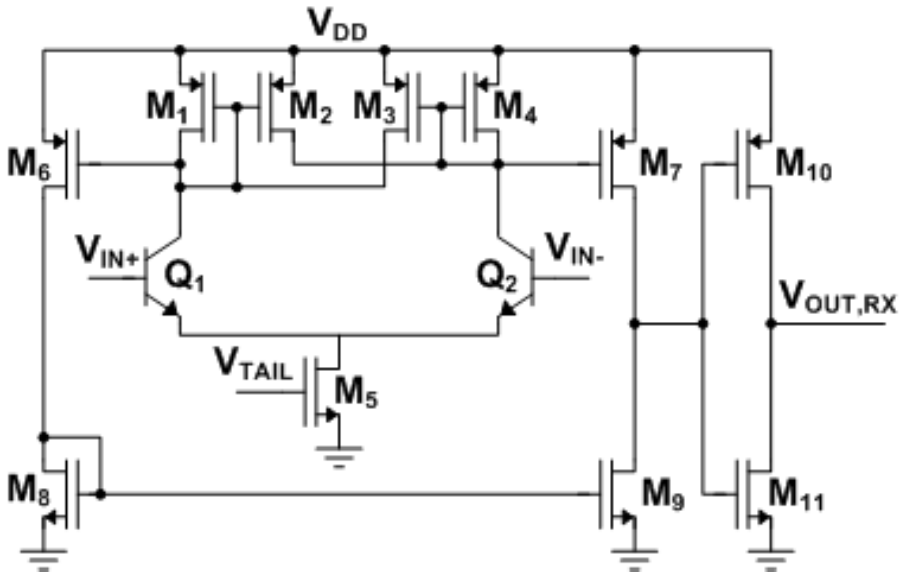

Figure 15: Reciever core topology with hysteresis. Positive feedback path notated in red.

and can be rearranged to find

$$V_{be,Q1} = \frac{kT}{q} \ln\left(\frac{I_{c,Q1}}{I_s}\right). \tag{8}$$

The trip point is defined by

$$V_{trip+} = V_{be,Q1} - V_{be,Q2}. \tag{9}$$

Substituting (8) into (9) and rearranging gives

$$V_{trip+} = \frac{kT}{q} \ln\left(\frac{I_{c,Q1}}{I_s}\right) - \frac{kT}{q} \ln\left(\frac{I_{c,Q2}}{I_s}\right) = \frac{kT}{q} \ln\left(\frac{I_{c,Q1}}{I_{c,Q2}}\right). \tag{10}$$

Finally, substituting (6) into (10) gives the intuitive form

$$V_{trip+} = \frac{kT}{q} \ln\left(\frac{(W/L)_{M3}}{(W/L)_{M4}}\right). \tag{11}$$

One may note from (11) that the hysteresis is proportional to temperature given these first order equations. As a result, an adequate ratio between $M3$ and $M4$ must be maintained to meet hysteresis requirements at -180°C, while balancing this against the necessary receiver sensitivity at high temperatures. A subsequent design

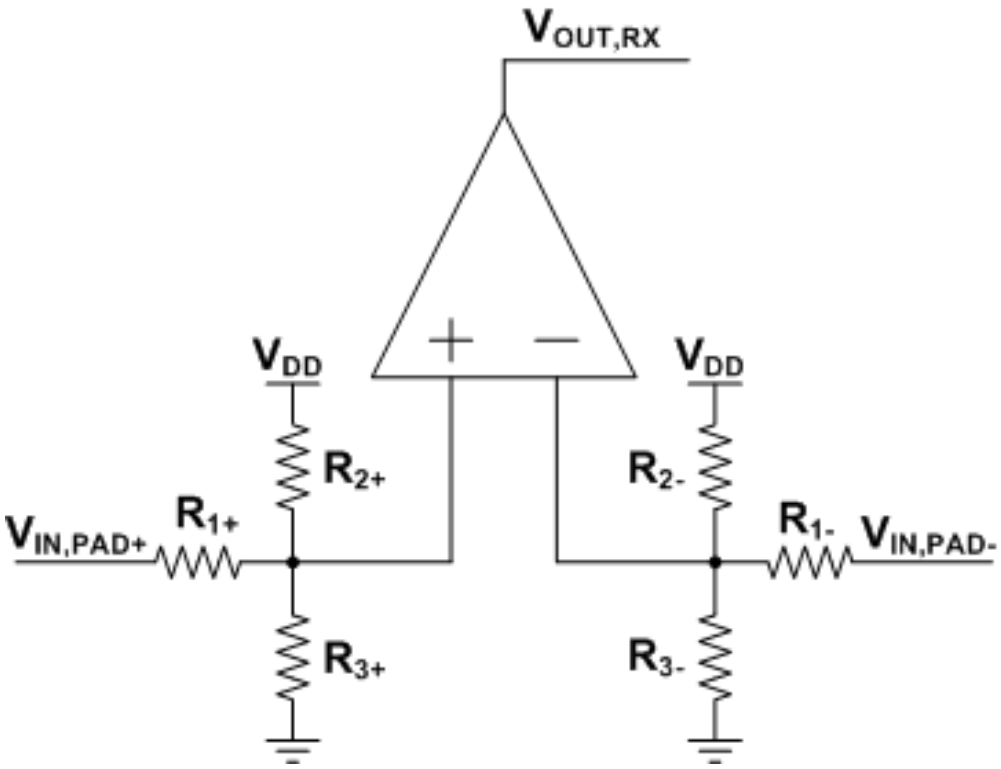

Figure 16: Input resistor network used to extend common-mode range beyond power supply rails.

was implemented to desensitize the hysteresis to temperature via positive resistive feedback from the output terminal. High sheet-resistance, lightly-doped polysilicon over DT resistors were used for the feedback.

The differential signal must also be compatible with a range of common-mode voltages, which is not necessarily suitable for the input range of a differential pair often used at the input of a comparator. To accommodate wide signal common-mode range, an on-chip resistive divider (Figure 16) was added at the input in order to level-shift the input to a valid range for the comparator. This technique results in reduced gain as the level-shifting process attenuates the input voltage. However, the comparator resolves the attenuated signal well due to the excellent gain of the HBT input pair. This can be related back to the exponential I-V relationship [4] observed in Gummel plot of Figure 2. One may note that the inputs to the receiver cannot

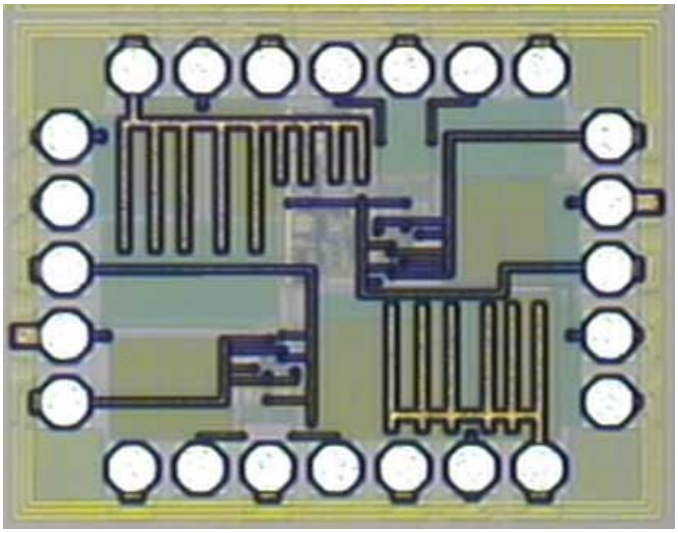

Figure 17: Receiver die photo.

have a typical ESD protection circuit because these clamp signal levels to within one diode drop of the upper and lower supplies (AVDD and GND in this case). Assuming that this part will be applied in a closed system and that the resistors at the input of the receiver afford some measure of ESD protection for the HBT input pair, ESD protected bond-pads have been omitted on the input pads. If signal levels are expected to be within the rail voltages – say for a robot with the same power supply rails and minimal voltage drop between parts – typical ESD protection diodes can be added back into the system to increase robustness. A further note, handling of the parts in testing for Section 2.8 did not show any susceptibility to ESD related failures. Though not exhaustive or covering worst-case ESD scenarios, that is a positive result.

As seen in Figure 15, an inverter buffer ($M10$ & $M11$) is incorporated at the output of the OTA comparator to help drive load capacitance encountered in testing. The target load was taken to be 5 pF, which turned out to be an optimistically small value as noted in Section 2.8. A revision to the receiver included a larger inverter buffer at the output to drive capacitive loads up to 70 pF representative of the test environment load.

Figure 17 shows the die photo of the first revision of the receiver. This was

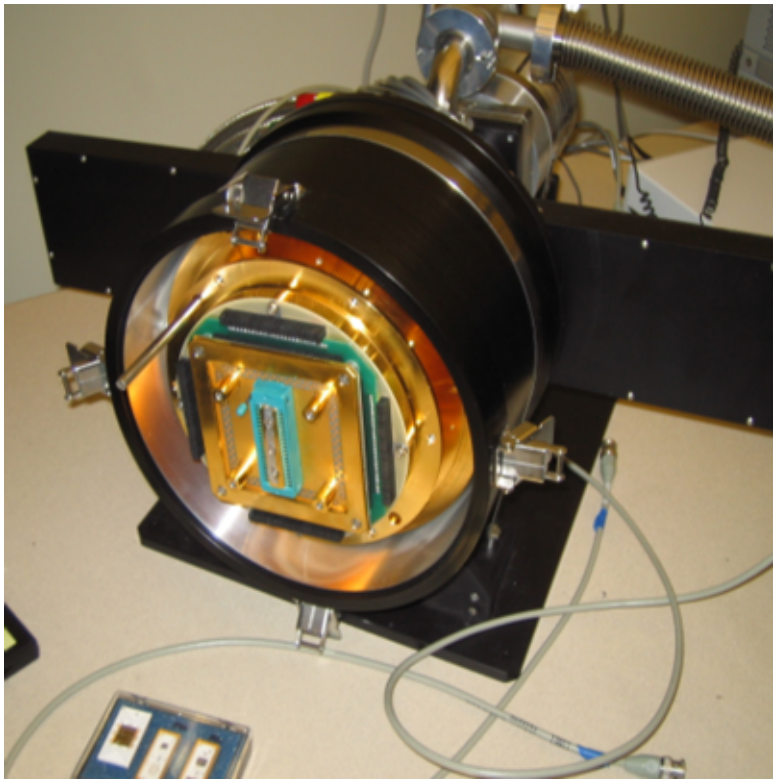

Figure 18: DC cryostat with DIP package adapter

designed to allow testing at the die level with GSGSG and GSG signal probes for the input and output respectively. Also, two versions of the receiver are included, one with internal current bias and the other with external current bias. The internal bias was a borrowed design, and reported data in following sections were taken with external bias to remove the variability of the internal bias.

2.6 Test Setup

Testing of the transmitter and receiver was done in a closed-cycle cryostat with built-in cooling capability as seen in Figure 18. The cryostat has temperature capabilities reaching down to 10 K. The cryostat accepts DIP style packages. So, the transmitter and receiver parts were bonded to 28 pin DIP packages for testing.

Keithley 2400 source meters were used to provide stable DC voltages and monitor the supply currents. The outputs of the transmitter were measured using a 500

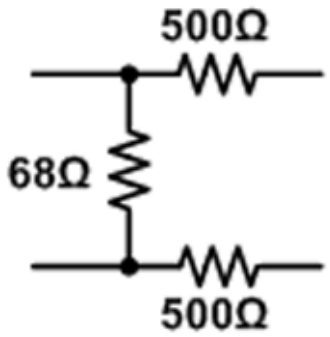

Figure 19: Transmitter termination board.

MHz Tektronix TDS7054 oscilloscope with selectable input impedance of either 50 Ω or 1 MΩ in parallel with 3 pF. Input waveforms were supplied by a Tektronix 3102 waveform generator. Initial testing showed that a proper output load and line termination would necessarily need to be applied to the transmitter to provide proper termination. The fast rising and falling edges of the transmitter output have high frequency content. High frequencies have a shorter wavelength which are on the order of the cable length used in testing, which leads to line bounce and reflections. These reflections corrupt the transmitted signal and consequently the measurements. As per the design of the transmitter, it was expecting to see a termination impedance around 60 Ω. So, a "termination" PCB (Figure 19) was designed to simultaneously provide a load to the transmitter of 68 Ω and prevent reflections at the oscilloscope input by enabling use of the 50 Ω input feature.

Measurement of the output of the receiver was also performed using the oscilloscope for rising and falling edges. For DC characteristics such as hysteresis, an Agilent 4155 was used. The time domain response of the receiver also proved to be tricky due to the parasitic load of the cables running between the package in the chamber and the test equipment outside the chamber. As packages were prepared, an on-package, series, "NP0" surface-mount capacitor was added to the receiver output to provide capacitive voltage division. This gave the effect of decreasing output load while also

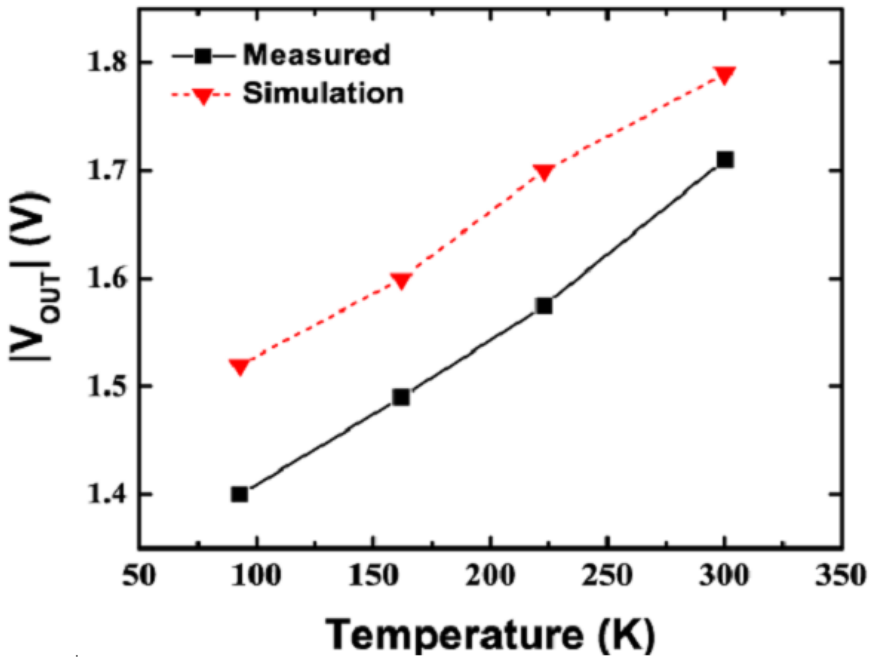

Figure 20: Transmitter single-ended output with termination board load.

decreasing the measured signal swing. While this method mitigates parasitic loading effects of the test setup, the measured output swing becomes a function of the temperature coefficient of the surface-mount capacitor.

2.7 Transmitter Test Results

Figure 20 shows the single-ended output voltage swing of the transmitter operating at temperatures of 300 K, 223 K, 163 K, and 93 K (-180°C). Simulated results are overlaid. As predicted in (2) and (3), the output swing is reduced by low temperatures. This can be traced to the thermally activated nature of $V_{BE,Q1}$, $V_{CE,Q2}$, and V_{D2}. At the lowest temperature point, the transmitter has a single-ended output swing of 1.4 V (2.8 V differential). This is below the desired specification of 3.0 V differential. However, under the circumstance of relatively short transmission distances seen in an exploratory vehicle, this is believed to be sufficient for the application. The measured results are within 125 mV of the simulated results across temperature.

Figure 21: Trasmitter input and differential output at 93 K.

Transient characteristics of the output waveform were measured differentially using the oscilloscope's math function to subtract single-ended signals. Sample inputs at 93 K and 300 K can be seen in Figures 21 and 22 respectively. In this testing setup, a noticeable "bounce" on the input can be seen, which is attributed to reflections between the function generator and transmitter input. Also, the output voltage does not have a one-to-one correspondence due to the voltage division from the transmitter output to the 50 Ω oscilloscope input.

Rise and fall times as well as propagation delays were determined from the oscilloscope waveforms (Figure 23). The propagation delay shows the expected temperature trend from simulation. This is expected because both peak f_T of the HBTs and CMOS inverter delays improve at low temperature. The rise and fall times, however, remain relatively invariant over temperature while simulations predicted that the edge rates would improve at low temperature. This discrepancy is believed to be related to a limit on the oscilloscope's sampling speed (rated only to 500 MHz).

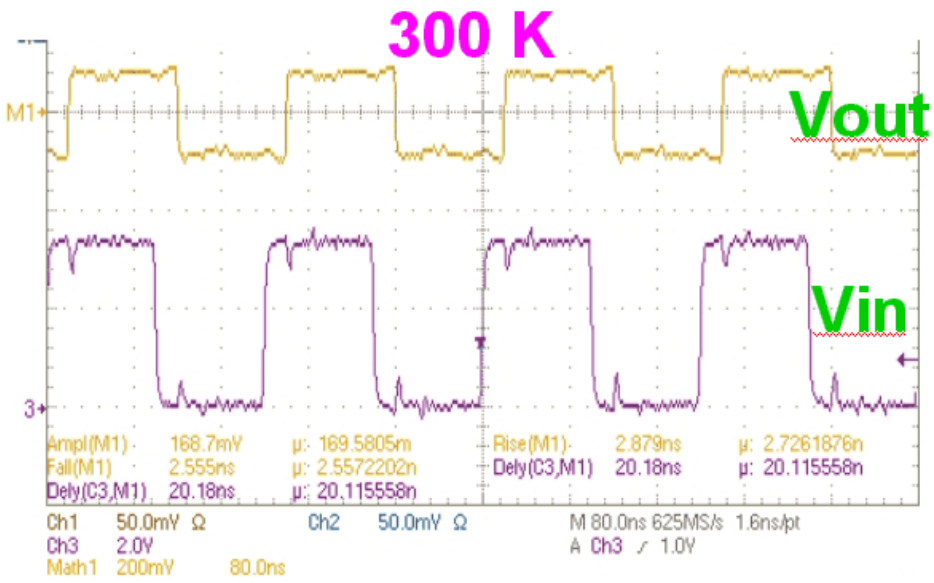

Figure 22: Trasmitter input and differential output at 300 K.

2.8 Receiver Testing

The hysteresis trip point for the original design was measured across temperature as seen in Figure 24. The trip point has a positive temperature coefficient of about 900 uV/°C as predicted by (11 and is overlaid on the plot. The difference between predicted and measured hysteresis can be linked to random mismatch between $Q1/Q2$ and $M1$-$M4$. The redesigned receiver incorporating resistive positive feedback is compared to the transistor feedback version in Figure 25. For the positive rising edge, resistive feedback shows much better stability with a slight negative temperature coefficient of approximately -68 uV/°C. However, the falling edge with resistive feedback has a much stronger temperature coefficient of approximately -435 uV/°C (an improvement over transistor feedback).

Input and output waveforms from the receiver can be seen at 300 K in Figure 26 and at 93 K in Figure 27. Some line bounce is observed, but this is believed to be due to the cables running from inside the cryostat chamber to the external connections in addition to a lack of termination resistors (receiver was not designed

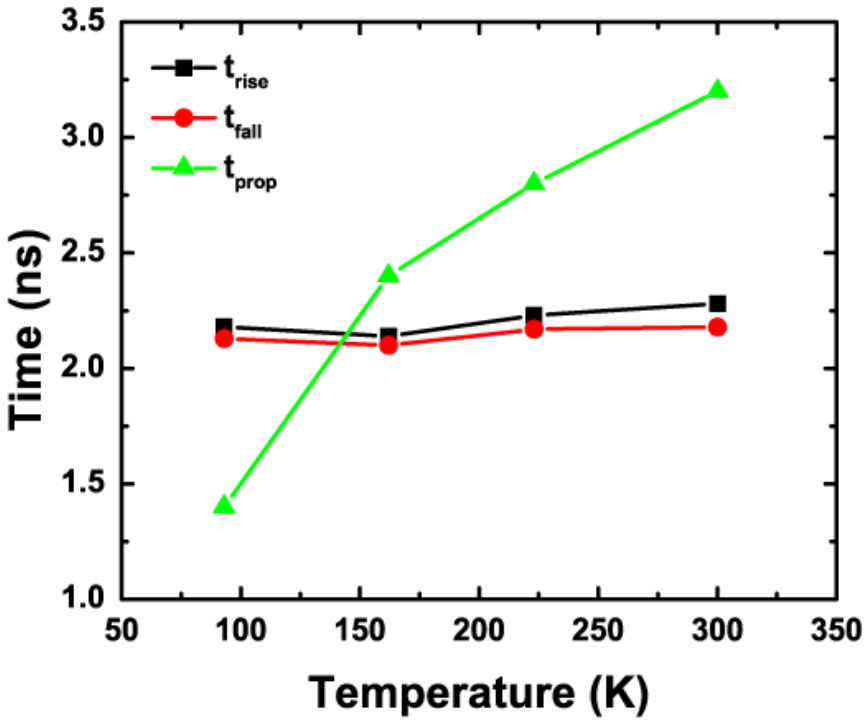

Figure 23: Measured rise/fall times and propagation delays for transmitter over temperature

to drive termination resistors). This observation is confirmed by the line bounce seen in the input signal which comes from an external function generator with excellent drive capability.

Transient performance measurements of the receiver are found in Figure 28. The propagation delay for the rising and falling edges both showed a decrease as temperature dropped. The rise and fall times were generally invariant, except for two spurious data points. As with the transmitter, no substantial change in edge times was expected.

2.9 Radiation Testing

Radiation testing of the transmitter and receiver hardware was performed under a 63 MeV proton beam at Crocker Nuclear Laboratory at the University of California at Davis. Parts were radiated at both 300 K and 77 K (-196°C). For 77 K, the parts were

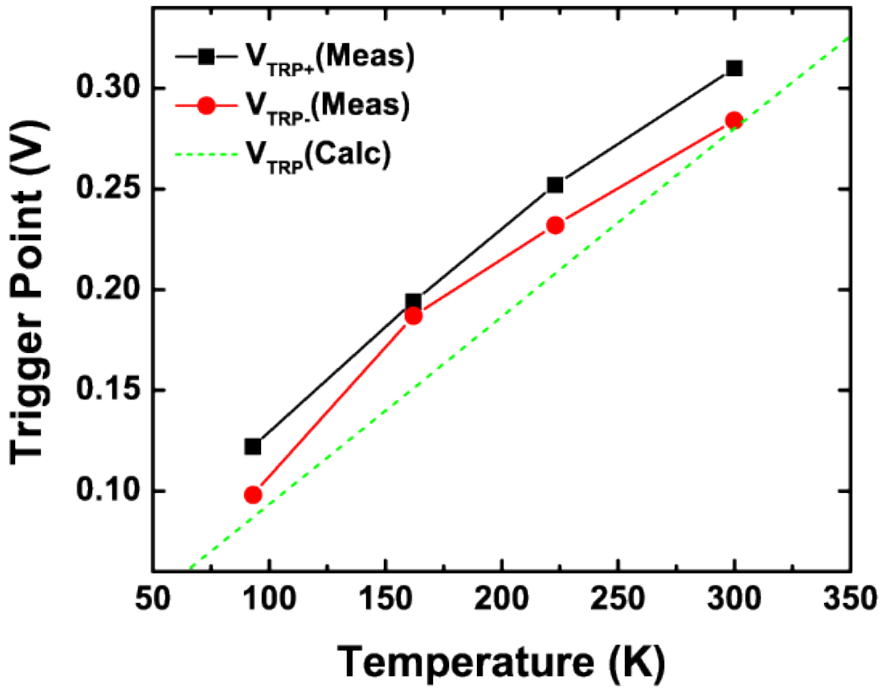

Figure 24: Receiver hysteresis measurements compared to calculated value across temperature.

mounted in a socket on a custom PCB and immersed vertically in a polystyrene dewar full of liquid nitrogen and placed in front of the beam outlet. The proton beam was operated at a dose rate of 1 krad(SiO_2)/s, and measurements were taken before radiation and then at total ionizing doses of 30, 60, 100, 300, 600, and 1000 krad(SiO_2). For both measurement temperatures, the transmitter and receiver were passing signal during radiation. Real-time monitoring of the transmitter and receiver supply current and output waveforms was performed via National Instruments LabVIEW software controlling the Keithley power supplies and Tektronix function generator and oscilloscope. This enabled data to be taken rapidly without delays due to entering the concrete bunker which houses the beam outlet. A picture of the set up may be seen in Figure 29.

Figure 30 shows the relative change in current for the transmitter output stage and driver stage power supplies at 77 K and 300 K. Because the power supplies were

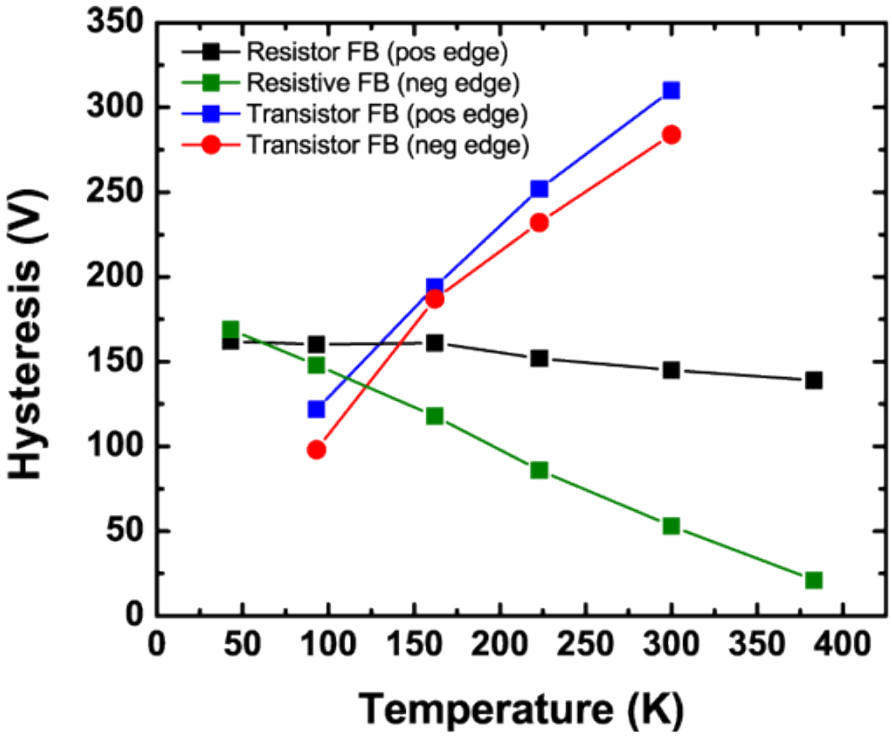

Figure 25: Comparison of hysteresis derived from resistive feedback and transistor feedback over temperature.

separately monitored, it is obvious that the output stage experienced only a slight current decrease of about 2 %. The output stage consists of only HBTs and Schottky diodes. So, at these radiation levels (≤ 1 Mrad), the HBTs show no measurable change in DC or AC performance (see Section 1.4). The driver stages, however, consist of both nFET and pFET devices in CMOS inverter configuration and in the output stage configuration seen in Figure 9. The nFET devices are expectedt to become leaky as a result of TID accumulation, and, therefore, the added current lines up with expectations. Transmitter propogation delay and rise/fall times were monitored throughout testing: no change was observed at 300 K or 77 K. The trasmitter was functional in testing up to 1 Mrad with no noticeable issues.

One receiver part was found to react oddly to exposure to the liquid nitrogen bath and to the radiation and consequently its operation failed prematurely. However, a second receiver part operated normally during testing. This part's relative rise/fall

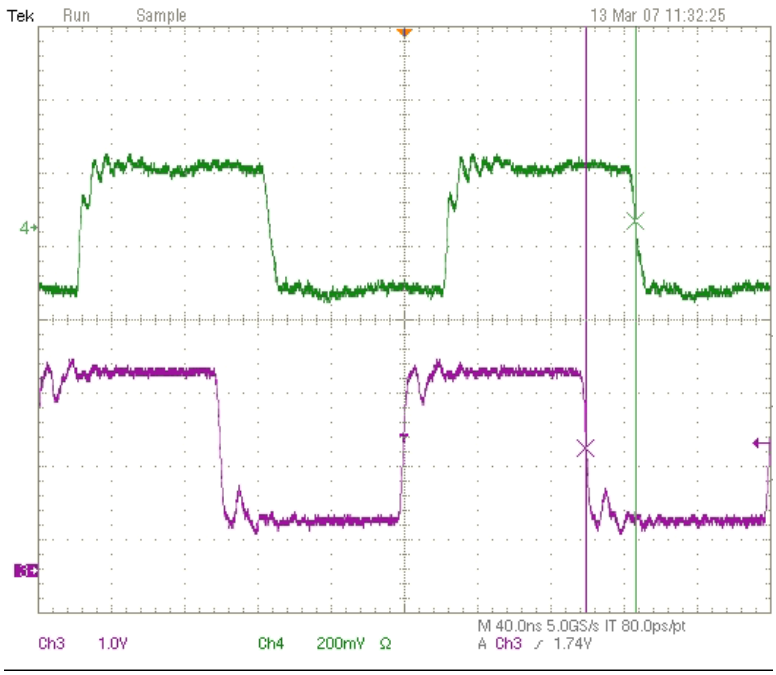

Figure 26: Receiver input (bottom) and output (top) waveform measured at 300 K.

times with respect to TID are shown in Figure 31. The receiver was observed to have little or no change in response to radiation at 300 K with TID up to 600 krad. However, at 77 K, a precipitous drop in the fall time of 27 % was observed. Data in [12] shows that the nFET devices exhibit slightly "off-state" leakage effects as a result of TID at 77 K than at 300 K. So, this may lead to stronger currents through the nFET devices and, therefore faster pull-down performance. During radiation testing, the receiver became unstable at 600 krad but was functional well beyond 100 krad, which is sufficient for the application. However, for environments with more TID, design should be carefully re-examined.

The voltage necessary to supply a 25 μA tail current to the nFET current mirror was also monitored. These data (Figure 32) show different response in the radiation response for 77 K and 300 K. Notably, the bias point changes much more dramatically at 77 K than at 300 K as little change was present at room temperature. This effect was observed in device-level radiation testing where the TID induced change in gate bias-voltage for a given current is more pronounced at 77 K than 300 K [12].

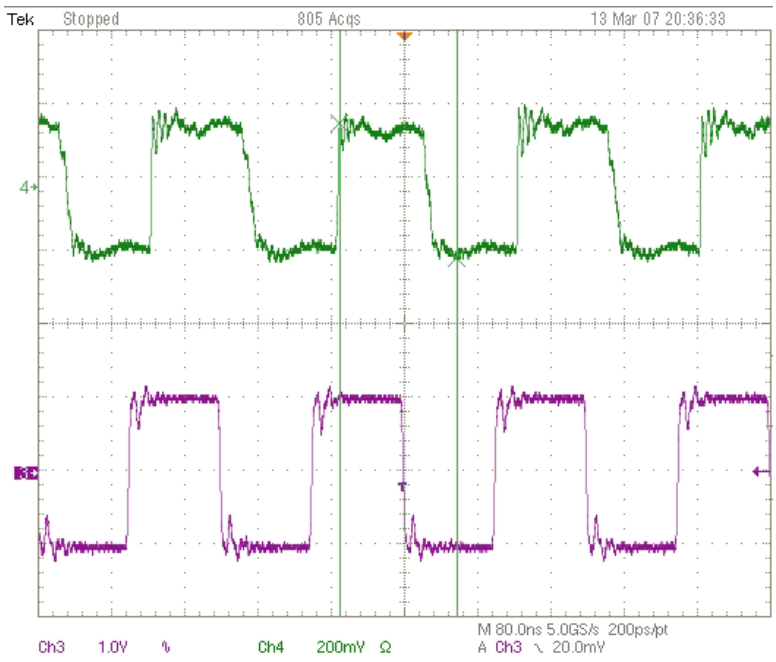

Figure 27: Receiver input (bottom) and output (top) waveform measured at 93 K (-180°C).

2.10 Summary

The specification, design, and testing of a RS-485 compatible transmitter and receiver (transceiver) have been discussed. The performance of the transmitter and receiver have been shown for liquid nitrogen temperatures (down to 77 K) and simultaneously under TID radiation (63 MeV proton irradition with TID of 300 krad). Some work on the layout of the transmitter and receiver is necessary to mitigate some single-event latch-up concerns and to reduce die area. Summaries of the measured performance for the transmitter and receiver are found in Table 3 and Table 4 respectively.

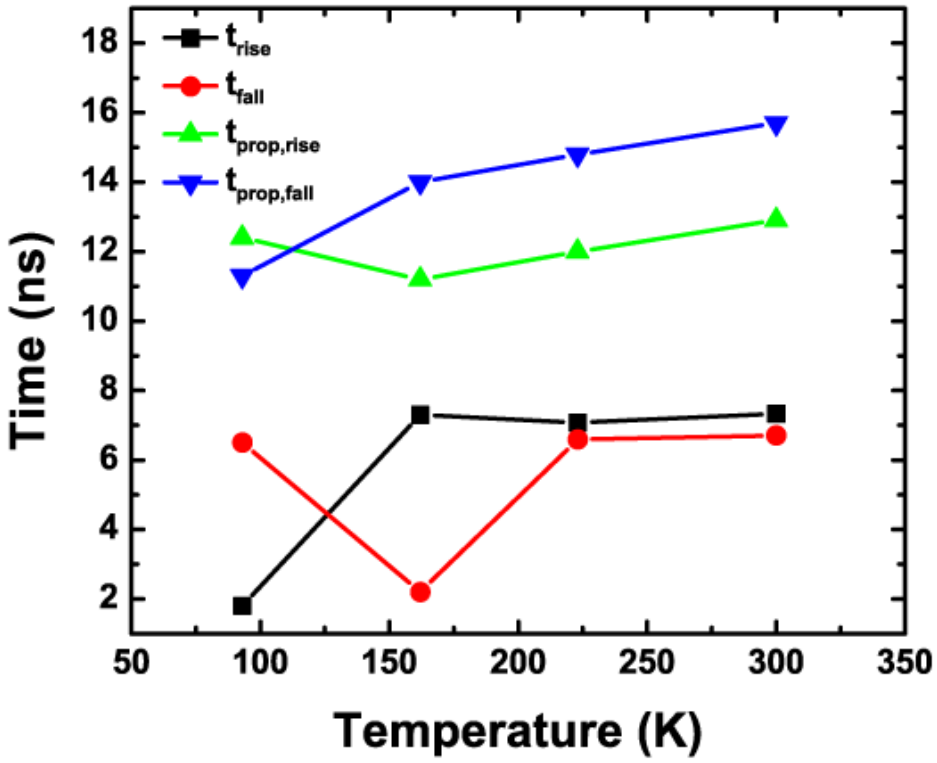

Figure 28: Receiver propogation delay, rise time, and fall time measured over temperature.

Table 3: Transmitter Measured Performance

Parameter	Performance	Unit
Output swing (single-ended)	> 1.40 V	
Rise/fall time	< 2.5	ns
Propagation delay	< 3.5	ns
Supply current (10 Mbps, R_L=68 Ω)	< 25	mA
Power (V_{DD}=3.3 V)	< 83 mW	
TID Tolerance	< 1	Mrad

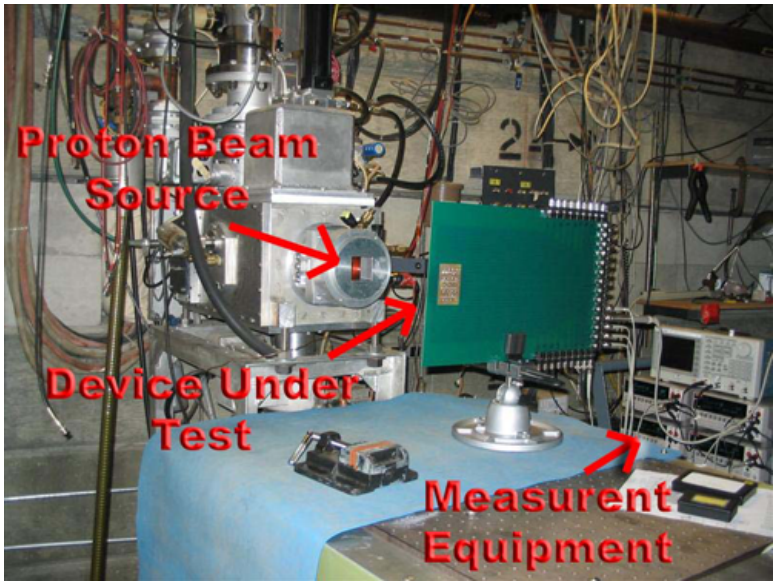

Figure 29: Test set up at Crocker Nuclear Lab at University of California Davis.

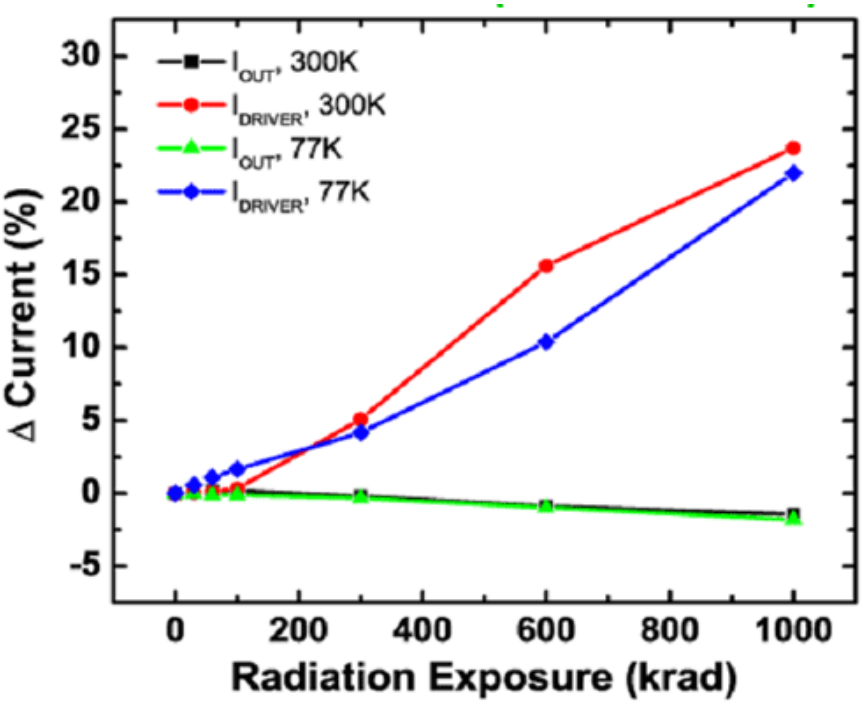

Figure 30: Transmitter performance under 63 MeV proton radiation with total ionizing dose up to 1 Mrad.

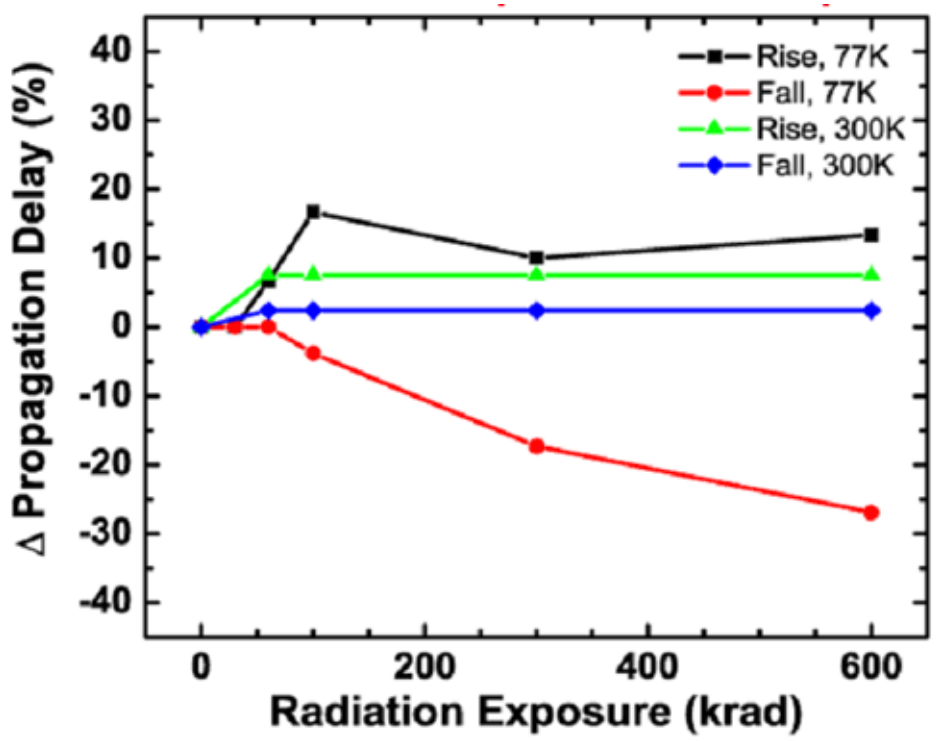

Figure 31: Receiver performance under 63 MeV proton radiation with total ionizing dose up to 600 krad.

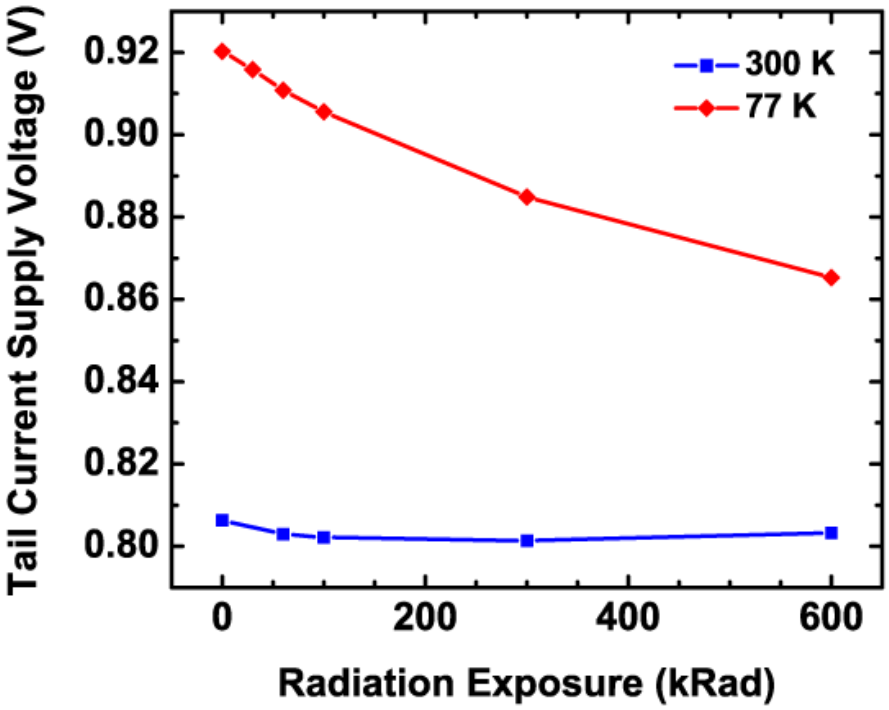

Figure 32: Measured voltage necessary to supply 25 μA tail current at 77 K and 300 K with radiation exposure.

Table 4: Receiver Measured Performance

Parameter	Performance	Unit
Rise/fall time	< 2.5	ns
Propagation delay	< 3.5	ns
Supply current (10 Mbps, $C_L \approx 5$ pF)	< 1.66	mA
Power (V_{DD}=3.3 V)	< 5.5	mW
Hysteresis (transistor FB)	> 95	mV
Input common-mode range	-3 to +6	V
Input resistance	> 100	kΩ

CHAPTER III

CHARGE AMPLIFICATION CHANNEL

3.1 Charge Channel Topology

The charge channel amplifier was designed to be an interface between a piezoelectric sensor and an ADC. A charge amplifier converts a charge stored on a capacitor to a voltage at its output. This allows the amplifier to measure and amplify signals from sensors in highly capacitive environments. For example, a piezoelectric sensor may be physically separated from the amplifier by several feet of highly capacitive cable. Given a voltage amplifier topology, the piezoelectric sensor would be required to drive the highly capacitive cable load in addition to the input of the voltage amplifier. Significant signal attenuation could occur for AC signals. On the other hand, a charge amplifier, Figure 33, responds to a charge deposited at its input by supplying an equal but opposite charge on the opposing side of a feedback capacitor to maintain voltage equality between the amplifier's positive and negative input terminals. Thereby a voltage is generated at the amplifier's output. This type of system is by nature insensitive to large values of C_{IN} as long as C_{IN} is not varying with time.

Assuming the simple example of Figure 33 with an ideal opamp, the input charge

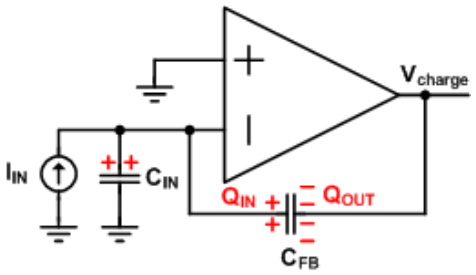

Figure 33: Charge amplifier in basic form with charge balance notated between the input and output.

can be related to the output charge and voltage by

$$\Delta Q_{IN} = -\Delta Q_{OUT} = -C_{FB}\Delta V_{OUT}, \tag{12}$$

or, more precisely,

$$\int_0^t I_{IN}(\tau)d\tau = -\int_0^t I_{OUT}(\tau)d\tau = -C_{FB}\left\{V_{OUT}(t) - V_{OUT}(0)\right\}. \tag{13}$$

The application of this charge channel amplifier requires some flexibility for operation with several different sensors. The specifications found in Table 5 call for operation with sensors that may supply up to 20,000 pC of charge at bandwidth of 5 kHz. The full-scale range of the 12 bit ADC was 1.2 V. [1] shows that the peak-to-peak quantization noise is equal to one LSB which may be determined by

$$LSB = \frac{V_{ref}}{2^N} = \frac{V_{range}}{2^N}. \tag{14}$$

This gives a quantization noise of 293 μV_{pk-pk} and sets the desired noise floor for operation of the charge channel.

Figure 34 shows the schematic of the charge amplification channel in total from sensor to output. Because the application provides only one supply, signals are referenced against 1.65, which is nominally $V_{DD}/2$ (more traditional designs have positive and negative rails with signals referenced against ground). An on-chip voltage reference based on the reference in [18] was used to generator a temperature stable

Table 5: Charge Channel Amplifier Specifications

Parameter	Min	Max	Unit
Supply voltage	3	3.6	V
Sensor charge output rating	200	20,000	pC
Signal bandwidth (upper)	100	5,000	Hz
Gain (2nd stage)	1	101	V/V
ADC input range	0	1.2	V
ADC resolution		12	bit
ADC quantization noise		293	μV_{pk-pk}

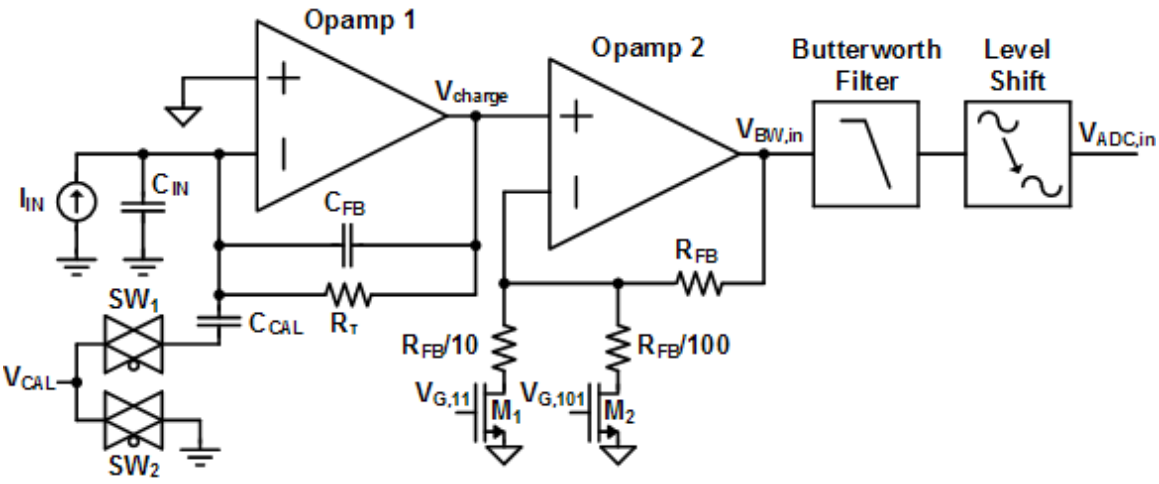

Figure 34: Charge amplification channel schematic including all signal-path components.

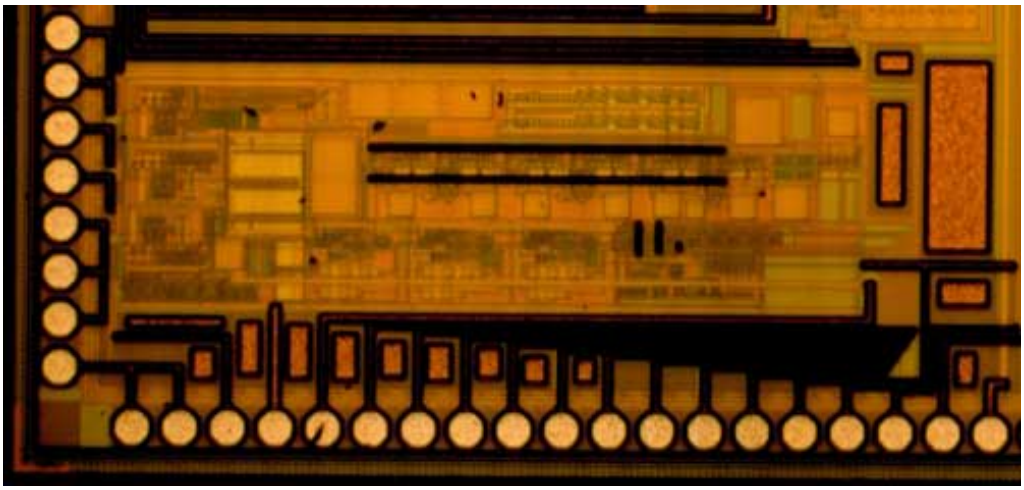

Figure 35: Die photo showing charge amplification channel.

reference of 1.65 V. The first opamp will be discussed in more detail in Section 3.2. Feedback capacitor C_FB was implemented off-chip due to its large size (∼33 nF) as was R_τ. A calibration signal, V_{CAL}, may be applied through CMOS switch SW_1 or grounded out through SW_2. The calibration signal is AC coupled through C_{CAL} which is a 100 pF MIM capacitor.

After input charge from the sensor is converted to a voltage, the voltage signal is applied to the input of opamp 2. This second stage is configured to provide three voltage-gain settings, A_V =1, 11, 101, which are switched via nFETs. Again, both

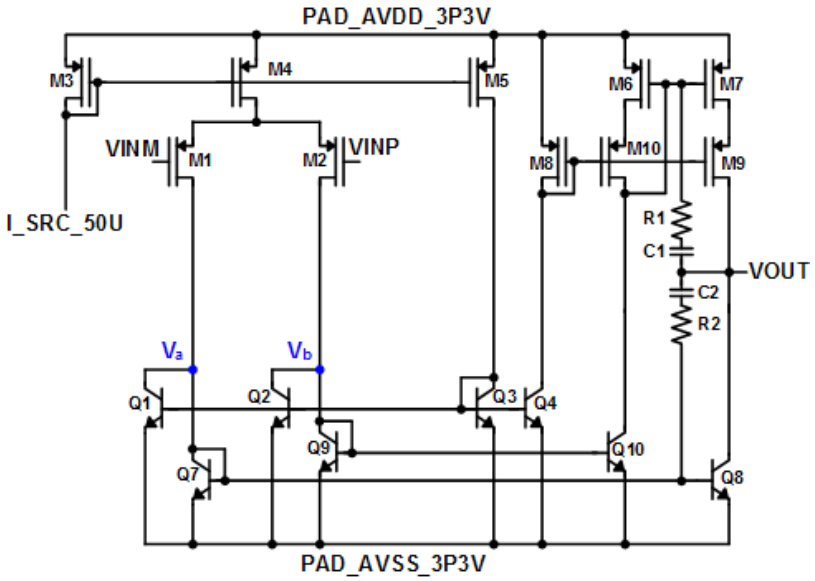

Figure 36: Charge channel front-end opamp schematic.

the input of opamp 2 and the shunt feedback resistors are referenced to $V_{DD}/2$. These signals are then passed through a 6th-order Butterworth switching filter to prevent aliasing within the ADC. The Butterworth filter bandwidth is controlled by the clock frequency supplied to the filter. This clock frequency, in actual application, will be supplied by a digital chip. Finally, the amplified and filtered signal is level-shifted and receives a small, inverting gain to match the input range of the ADC. Figure 35 is a die photo of the channel from input to the output of the level-shifter.

3.2 Charge Channel Front-end Opamp Design

The front-end opamp has several design constraints. First, the input bias current must be minimal since the amplifier is used to sense and integrate small amounts of charge. This precludes the use of HBTs at the input due to their finite base bias current. Therefore, either pFETs or nFETs had to be employed at the input. pFETs were selected due to their superior TID radiation tolerance (see Section 1.4). The opamp needs to be able to slew a 33 nF capacitor at a sufficient rate to meet signal bandwidth requirements while being stable in a feedback configuration. With such

large capacitances being employed, having the dominant pole at the output node appears to be a safe choice. So, we arrived at an output transconductance topology where the positive and negative transconductance signals are combined at the output. Figure 36 shows the topology actually used in this design.

Next, the noise injected into the signal path needs to remain under the quantization noise of the ADC in order to maintain the LSB of the ADC. Input referred noise from the first opamp is directly affected by the gain in its internal stages. To minimize noise from the output node, the gain from the input stage needed to be maximized. The voltage gain from the input to the node $V_{a/b}$ is approximately

$$\frac{V_{a/b}}{V_{IN,-/+}} = \frac{g_{m,M1/2}}{g_{m,Q7/9}}. \tag{15}$$

Noting that $g_{m,M1/2}$ is by definition $\partial I_{DS,M1/2}/\partial V_{GS,M1/2}$, we know that

$$g_{m,M1/2} = \sqrt{2K' \left(\frac{W}{L}\right)_{M1/2} I_{DS,M1/2}}. \tag{16}$$

Clearly, increasing $I_{DS,M1/2}$ improves $g_{m,M1/2}$, but we also know that

$$g_{m,Q7/9} = \frac{I_{C,Q7/Q9}}{V_t}. \tag{17}$$

Noting the structure of an OTA input stage, we can equate $I_{DS,M1/2}$ with $I_{C,Q7/9}$. So, substituting (16) and (17) into (15) gives an expression for the first stage gain of

$$\frac{V_{a/b}}{V_{IN,-/+}} = \frac{\sqrt{2K' \left(\frac{W}{L}\right)_{M1/2} I_{DS,M1/2}}}{\frac{I_{C,Q7/8}}{V_t}} = \frac{V_t \sqrt{2K' \left(\frac{W}{L}\right)_{M1/2}}}{\sqrt{I}}. \tag{18}$$

Unfortunately, with a simple OTA, increasing current in the first stage actually hurts gain, but this effect can be side-stepped if a shunt leakage path, hence $Q_{1/2}$. These transistors, allow the current through $M_{1/2}$ to be controlled separately from $Q_{7/9}$.

By increasing the current in the first stage with the topology shown in Figure 36, the noise contributions of components in the output summing nodes are decreased. However, FET devices are notorious for a substantially higher $1/f$ noise corner frequency as compared to their HBT counterparts [16]. Given the low frequency nature

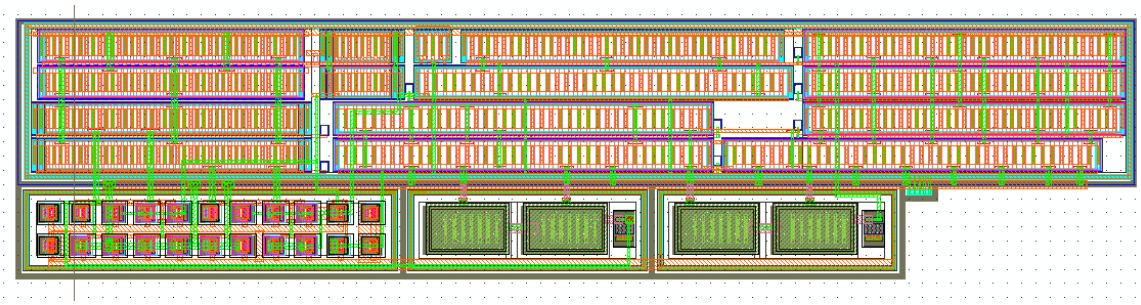

Figure 37: Charge channel front-end opamp layout with dimensions of 396 x 92 μm^2.

of this system, the $1/f$ noise is not desirable, and this did pose a significant threat to overall noise performance. Based on design kit modeling data and knowledge about the dependency of $1/f$ noise on gate area [28], the input pFET W×L was enlarged. Of course, this has a negative impact by moving the input pole to lower frequency. However, with the targeted bandwidth of around 5 kHz and the low-frequency pole at the output, this effect does not have any major impact on channel operation.

The amplifier also needs to have minimal offset due to the DC-coupled nature of the system. Any offset in the opamp gets multiplied by the voltage gain of the amplifier stages before reaching the input of the ADC and can cause the system to "rail," especially in high-gain mode. Systematic offset is a result of any error between the positive and negative stages. In this design, the largest source of systematic offset is from the collector nodes of $Q8$ and $Q10$ having different nominal voltages. Namely, the collector of $Q10$ sits at one V_{GS} below AVDD, but the collector of $Q8$ will typically be at the common-mode level (nominally 1.65 V for this application). So, this introduces a systematic offset that can be reflected to the input: around 1.3 mV at room temperature in simulations. This systematic offset could be improved by cascoding $Q8$ and $Q10$ with nFETs that would shield the collectors from the output voltage change. This comes at the expenses of some layout area, extra current for biasing the transistors, and headroom at the output (reduced by a V_{DS}). By placing nFET devices as cascode devices, there is believed to be little change in performance

due to any TID values since the current mirror from Q_7 to Q_8 or Q_9 to Q_{10} is dominated by the "g_m device"—in this case, TID tolerant HBTs. This could be a future design change. [25, 28].

Random mismatch for this circuit is rather more troubling than systematic offset. Mismatch between the input devices leads to offset in the circuit. FETs are known to be inferior to HBTs in terms of random mismatch due to their sensitivity to variation of gate dimensions (affects K) and oxide thickness (affects threshold voltage). HBTs, on the other hand, are much less sensitive since their vertical profile determines device parameters. These parameters are typically very well controlled, especially as devices are placed in close proximity.

The pFET devices at the input have a rather large size as designed (40 fingers of $\frac{10\ \mu m}{1\ \mu m}$ for an effective width of 400 μm), which helps to reduce the mismatch between gate dimensions. However, the size of the input pair cannot be increased much more without negatively effecting stability response and overall amplifier size, especially since the random mismatch of the input pair only improves by the square root of

Table 6: Simulated Front-end Opamp Electrical Characteristics

Parameter	-180°C	+25°C	+125°C	Unit
Unity-gain bandwidth (C_L = 33 nF)	109	65	55	kHz
3dB bandwidth (C_L = 33 nF)	33	65	33	Hz
DC gain	70	67	64	dB
Phase margin (C_L = 33 nF)	89	89	89	deg
Systematic offset in unity-gain configuration	0.45	1.29	1.84	mV
Positive/negative slew rate (C_L = 33 nF)	45/-56[1]	57/-52	46/-53	kV/s
Positive-going error while integrating 100 μA current (C_{FB} = 33 nF)	0.94	0.94	0.92	%
Negative-going error while integrating 100 μA current, (C_{FB} = 33 nF)	0.79	0.78	0.77	%
Quiescent current ($V_{IN,CM}$ = 1.65 V)	880	1004	1041	μA
Quiescent power ($V_{IN,CM}$ = 1.65 V and V_{DD} = 3.3 V)	2.64	3.01	3.12	mW

gate area To enable the opamp to be used in an application other than the front-end opamp, it was designed with sufficient internal compensation for a unity-gain feedback configuration. This was achieved by the addition of C_1, C_2, R_1, and R_2.

Table 6 provides a summary of the simulated performance of the opamp at three temperature points with a 33 nF load typical of its intended application. A screen capture of the layout can be seen in Figure 37. The circuit layout was intentionally kept compact with circuit dimensions of 396 x 92 μm^2. The pFET devices were kept completely separate from the npn HBT devices by intervening substrate contacts, deep trench isolation, and n-well contacts. The result is a structure which should be resistant to SEL effects. At the same time, by keeping the circuit compact, one hopes to reduce mismatch due to spacing between components. [32] provides an interesting study of FET mismatch somewhat contrary to text-book knowledge: common-centroid (a.k.a. cross-coupled) type architecture does not necessarily provide benefits in mitigating device mismatch. So, space was conserved by maintaining close-proximity and optimal routing for space. From Monte Carlo simulations with 100 data points, one standard deviation on the opamp's input-referred offset at 300 K was determined to be 2.3 mV.

3.3 Charge Channel Testing

The charge channel was tested in an open-cycle cryostat with a bandwidth capability of at least 100 MHz. AVDD and DVDD were supplied by separate Keithley 2400 sources. The Tektronix TDS7054 oscilloscope was used to measure appropriate signals in addition to a Keithley digital multimeter (for DC measurements). A Keithley 6221 DC and AC current source was used to simulate the sensor at the input. This source has the capability of providing variouis wave current input signals than can in turn be integrated by the charge channel. It should be noted that the current source used has accuracy to the 4th significant digit, which may affect some results due to the

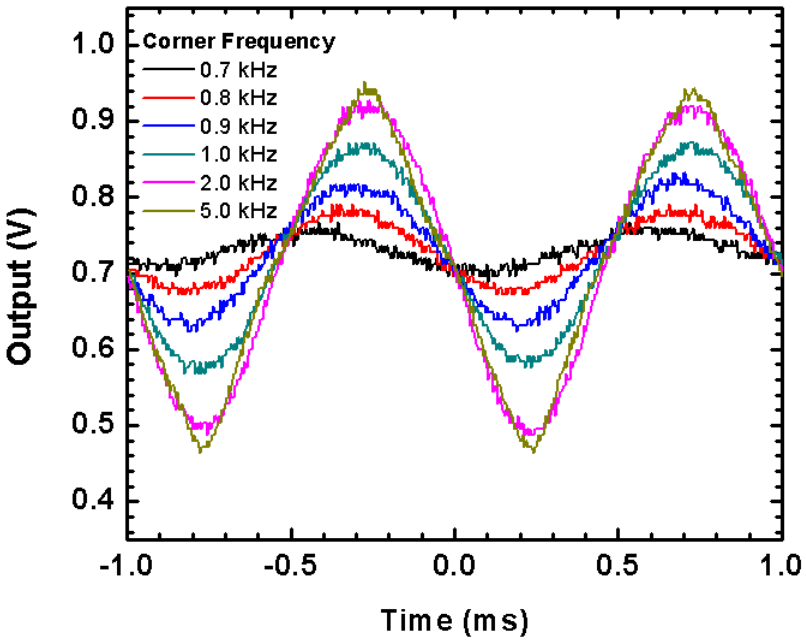

Figure 38: Charge channel integrating 1 kHz square wave with varying Butterworth filter corner frequency at 393 K.

sensitivity of the charge channel to small charges. For example, when operating in the 20 uA range, the current source may have offset or inaccuracy as large as 1 nA [14].

Figure 38 shows the output of the charge channel while integrating a 1 kHz, 20 uA square wave. The Butterworth filter corner frequency was changed by reducing the clock frequency from 500 kHz down to 70 kHz. Clearly, reducing the clock frequency reduces the corner frequency and filters out the harmonics of the expected triangle-wave output leaving only a small portion of the fundamental when the Butterworth clock is set to 70 kHz. This was repeated across several temperature points. Figure 39 shows the same result taken at 93 K (-180°C).

Measurements were also taken with the amplifier in the medium gain mode (A_v = 11). Figure 40 and 41 shows the amplifier operating with a 1 kHz, 2 μA signal at the input. Clearly, there is some offset in the circuit, which was observed to vary if

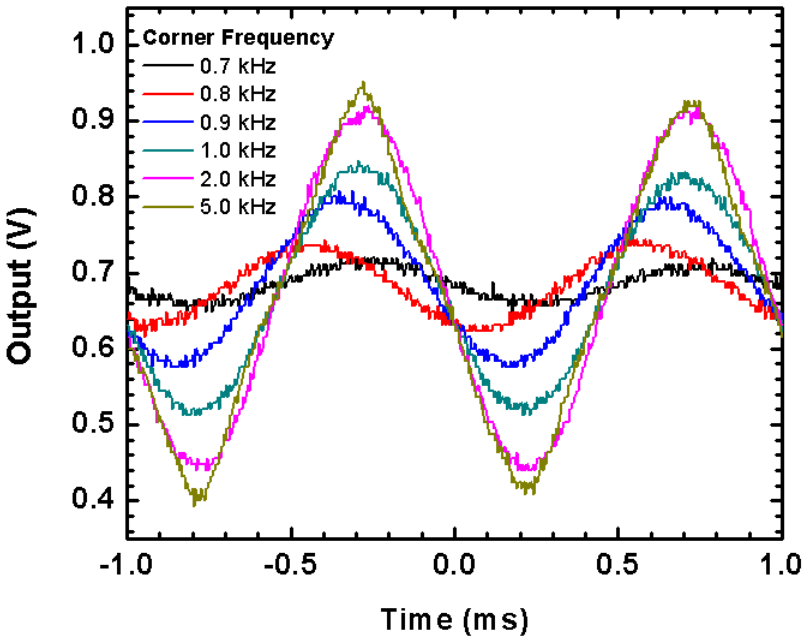

Figure 39: Charge channel integrating 1 kHz square wave with varying Butterworth filter corner frequency at 093 K.

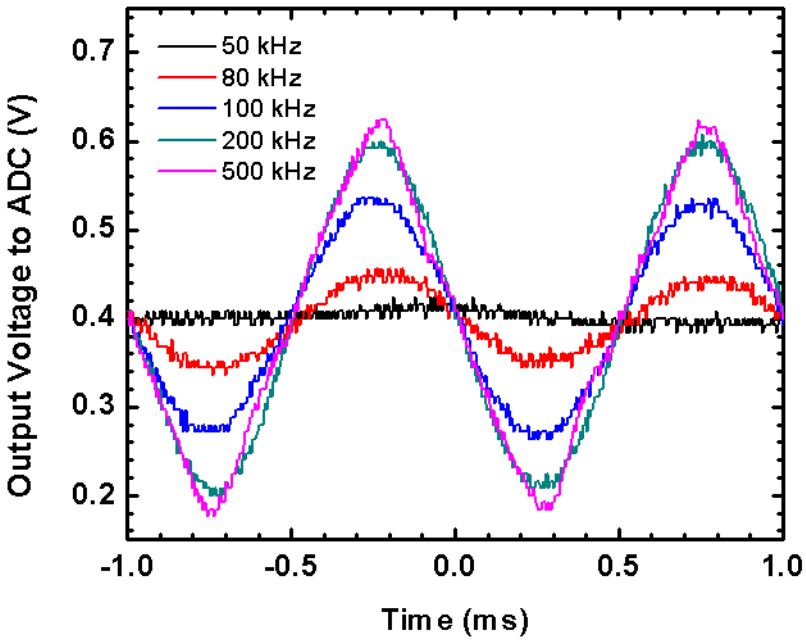

Figure 40: Charge channel operating with medium gain ($A_v = 11$) while integrating 1 kHz, 2 μA square-wave at 393 K.

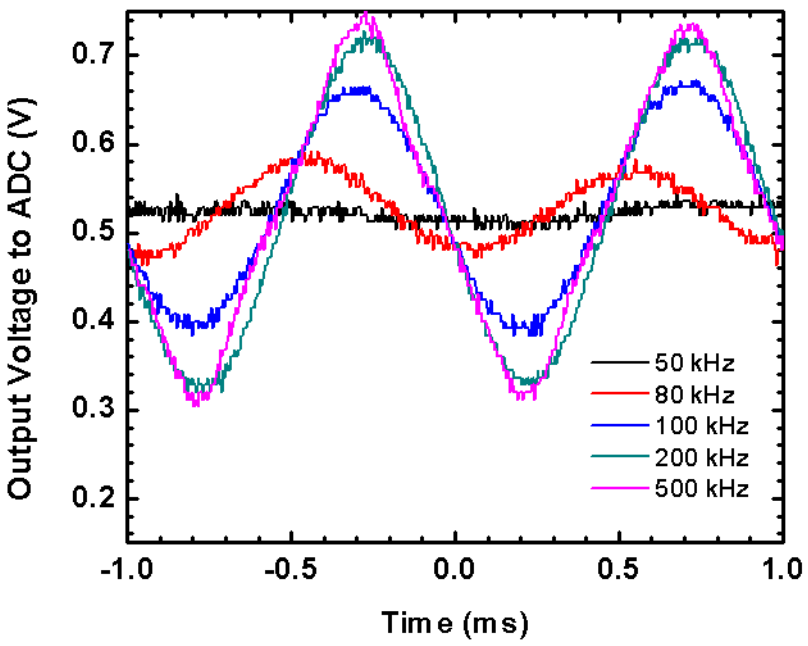

Figure 41: Charge channel operating with medium gain ($A_v = 11$) while integrating 1 kHz, 2 μA square-wave at 163 K.

the current source at the input was removed from the circuit in addition to varying with the circuit's temperature.

Investigation into the offset see in Figures 40 and 41 revealed a much worse scenario in the high-gain mode: the channel output to the ADC and the signal level at the input to the Butterworth filter were observed to be railing. Measurements of the offset voltages of the 1st and 2nd opamps at room temperature revealed that the actual offset in these opamps were close to the 3σ value as determined by Monte Carlo simulations. For the 1st opamp (shown in Section 3.2), the offset was observed to be 6, 6, & 8 mV for three parts. The 2nd opamp, whose design is not here-in discussed, had measured offset of 8, 9, & 10 mV for the same respective measurements in the 1st opamp. A revision was performed to allow the offet to be "dialed-out" by adding a pad that interfaces the 2nd opamp's inverting terminal. As a result, for interim testing purposes, this will allow the charge amplification channel to be operated in

high-gain mode and medium-gain mode with significant DC offset being present at the input to the Butterworth filter

3.4 Conclusions

The charge amplification channel was designed, fabricated, and tested. Further investigation into the DC offset that was observed will be necessary to eliminate its unwanted effects in the medium- and high-gain modes. It is suggested that auto-zeroing opamps be considered due to their reduced $1/f$ noise and substantially reduced DC offset performance. Nevertheless, a system-on-package design has been demonstrated that amplifies an input charge, filters out harmonics to prevent aliasing, and can serve as an interface between a piezoelectric sensor and an ADC.

CHAPTER IV

LOW-IMPEDANCE OUTPUT BUFFER

4.1 Motivation

Amplifiers designed for implementation in a fully integrated system typically have a limited ability to drive low-impedance loads. One such example is the opamps designed for the charge channel. So, an output buffer was designed with the ability to drive a 50 Ω oscilloscope load in mind.

4.2 Topology Selection

The simplest topology explored was a simple emitter follower (Figure 42). This topology is well known for its relatively low output and fairly high input impedances. The small signal DC input resistance is

$$R_{in} = r_\pi + (Re\{Z_L\} \parallel r_o)(\beta + 1). \tag{19}$$

The small signal output impedance is found to be

$$R_{out} = \frac{r_\pi + R_S}{\beta + 1} \parallel r_o. \tag{20}$$

However, an emitter follower has a gain given by

$$A_V = (\frac{R_{in}}{R_{in} + R_S}) \cdot g_m \cdot (\frac{1}{g_m} \parallel R_L \parallel r_o). \tag{21}$$

A notable feature of the emitter-follower gain is that it is significantly reduced by the R_L term as the load impedance approaches $1/g_m$. Therefore, a simple emitter follower has undesirable DC gain characteristics, which are further degraded by changes in g_m as the output voltage changes in large-signal swing. This leads to large signal distortion.

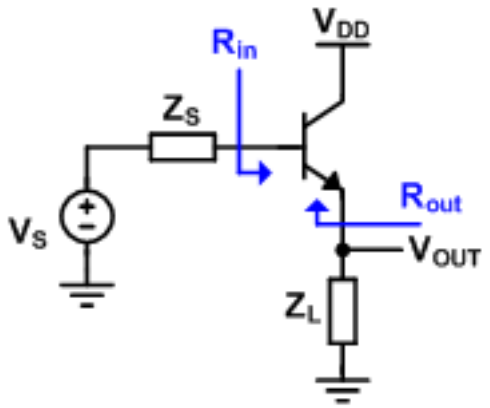

Figure 42: Basic emitter follower topology.

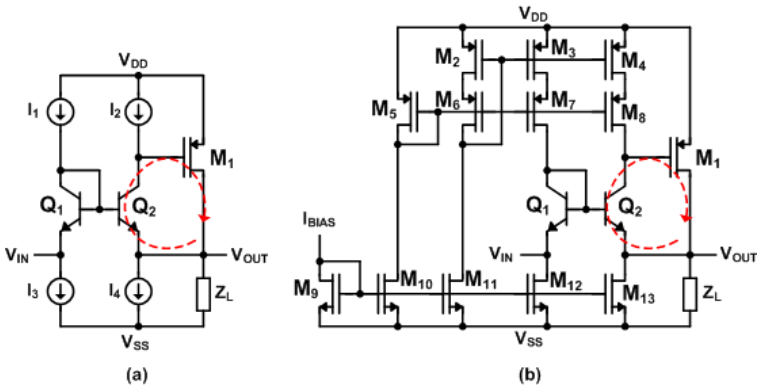

Figure 43: Output buffer incorporating shunt feedback (red dashed-line): (a) shows the core circuit while (b) gives the full circuit topology.

So, in order to provide voltage gain less dependent on $g_{m,Q2}$ and Z_L, the topology seen in Figure 43a was explored. This topology employs shunt-feedback at the output in order to reduce sensitivity to load impedance and bias point. The feedback path starts at V_{OUT} and then moves from the emitter to the collector of $Q2$ and gate of $M1$. pFET $M1$ provides signal inversion from gate to drain, which is again V_{OUT}. A practical implementation of the circuit is found in Figure 43b.

4.3 Signal Range

Input signals see the emitter of $Q1$ which is diode connected. $Q1$ acts like a floating diode between two high impedance nodes level-shifting the input signal up to the base

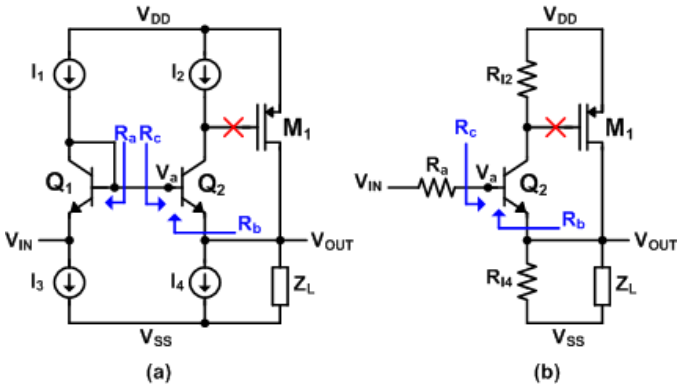

Figure 44: Super follower input and output impedance assumptions and calculations.

of $Q2$. Signal is then level shifted to the output through the base-emitter junction of $Q2$. The maximum input voltage where regulated voltage gain occurs is found to be limited by transistors $Q1$ and $M1$ related by

$$V_{IN,max} = V_{DD} - V_{GS,M1} - V_{BE,Q1}. \tag{22}$$

The minimum regulated input voltage is limited by current source $I3$ ($M12$) to

$$V_{IN,min} = V_{SS} + V_{DS(sat),M12}. \tag{23}$$

4.4 Small-Signal Analysis

Applying small-signal analysis is useful to find the sensitivities of the buffer design. First, the feedback loop should be broken to enable calculation of open-loop resistances as shown by the red "X" in Figure 44a.

The resistance R_b can be derived by making a few assumptions seen in Figure 44b. First, as stated above, the impedance of diode-connected $Q1$ is assumed to be much less than the impedance looking into I_1 and I_3. This greatly simplifies the connection to the input, which is then taken to have resistance R_a. The small signal model leads to

$$R_a = \frac{r_{\pi,Q1}}{\beta_{Q1}+1} \parallel r_{o,Q1} = \frac{1}{g_{m,Q1}} \parallel r_{\pi,Q1} \parallel r_{o,Q1} \approx \frac{1}{g_{m,Q1}}. \tag{24}$$

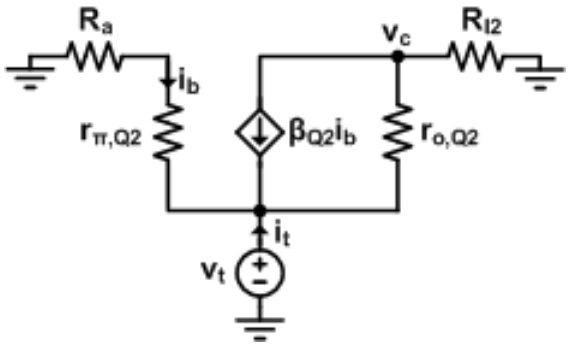

Figure 45: Small signal model for calculation of R_b.

With R_a having been found, R_b as seen in Figure 44 can be determined applying a test source, V_t, to the small signal model in Figure 45. R_b is then given by

$$\frac{v_c}{R_{I2}} + \frac{v_c - v_t}{r_{o,Q2}} + \beta_{Q2} i_{b,Q2} = 0, \tag{25}$$

$$i_t + i_{b,Q2} + \beta_{Q2} i_{b,Q2} + \frac{v_c - v_t}{r_{o,Q2}} = 0, \ and \tag{26}$$

$$\frac{-v_t}{R_a + r_{\pi Q2}} = i_{b,Q2}. \tag{27}$$

Solving (25) for v_c and substituting into (26) and (27) yields

$$v_c = (\frac{v_t}{r_{o,Q2}} + \frac{\beta_{Q2} v_t}{R_a + r_{\pi,Q2}})(R_{I2} \parallel r_{o,Q2}), \ and \tag{28}$$

$$i_t = \frac{v_t(1+\beta_{Q2})}{R_a + r_{pi,Q2}} + \frac{v_t}{r_{0,Q2}} - \frac{v_c}{r_{o,Q2}}. \tag{29}$$

Finally, eliminating v_c from 28 and 29 and rearranging yields the desired resistance

$$R_b = \frac{v_t}{i_t} = \frac{R_a + r_{pi,Q2}}{1+\beta_{Q2}} \parallel \frac{r_{o,Q2}}{1 - \frac{R_{I2} \parallel r_{o,Q2}}{r_{o,Q2} \parallel \frac{R_a + r_{\pi,Q2}}{\beta_{Q2}}}}. \tag{30}$$

One final simplification may be made assuming $r_{o,Q2} \gg \frac{R_a + r_{pi,Q2}}{1+\beta}$ which gives the back-of-the-envelope resistance of

$$R_b \approx \frac{R_a + r_{\pi,Q2}}{1+\beta_{Q2}} \overset{R_a \ll r_{\pi,Q2}}{\longrightarrow} \frac{1}{g_{m,Q2}}. \tag{31}$$

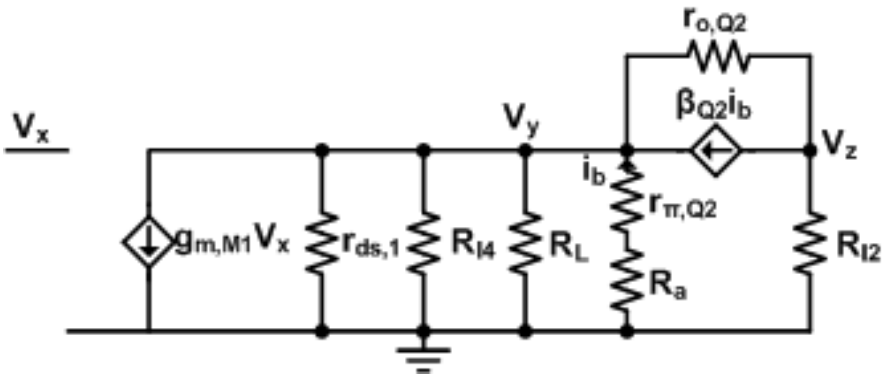

Figure 46: Small-signal model for calculating feedback loop gain.

From [9], the open-loop input impedance looking into Q_2 was determined to be

$$R_c = r_{\pi,Q2} + (\beta_{Q2}+1)R_e\left(\frac{r_{o,Q2}+\frac{R_{I2}}{\beta_{Q2}+1}}{r_{o,Q2}+R_{I2}+R_e}\right), \tag{32}$$

where $R_e = r_{ds,M1} \parallel R_{I4} \parallel R_L$.

Next, the loop gain for the feedback path needs to be determined. The feedback path is broken at the gate of $M1$ for calculations. The small signal model for finding the loop gain is found in Figure 46. Summing the currents at node V_z, one finds

$$\frac{V_z}{R_{I2}} + \beta_{Q2}i_{b,Q2} + \frac{V_z}{r_{o,Q2}} - \frac{V_y}{r_{o,Q2}} = 0. \tag{33}$$

By inspection, base current of $Q2$ can be related to voltage V_y by

$$i_{b,Q2} = \frac{-V_y}{r_{pi,Q2}+R_a}. \tag{34}$$

Substituting (34) into (33) and re-arranging, the voltage gain from V_y to V_z is found to be

$$\frac{V_z}{V_y} = \frac{\frac{1}{r_{o,Q2}}+\frac{\beta_{Q2}}{r_{\pi,Q2}+R_a}}{\frac{1}{R_{I2}}+\frac{1}{r_{o,Q2}}} = (R_{I2} \parallel r_{o,Q2})\left(\frac{1}{r_{o,Q2}}+\frac{\beta_{Q2}}{r_{\pi,Q2}+R_a}\right) = A_{y\to z}. \tag{35}$$

Though thorough, (35) does not provide much intuition. Assuming that $r_{o,Q2} \gg \frac{r_{pi,Q2}+R_a}{\beta_{Q2}}$, the voltage gain becomes

$$\frac{V_z}{V_y} = A_{y\to z} \approx (R_{I2} \parallel r_{o,Q2})\left(\frac{\beta_{Q2}}{r_{\pi,Q2}+R_a}\right). \tag{36}$$

A sanity check agrees that (36) is of the familiar form $G_m R_{OUT}$ if $R_a \ll r_{\pi,Q2}$ and the load at the collector of $Q2$ is $R_{I2} \parallel r_{o,Q2}$.

Now, let $R_e = r_{ds,M1} \parallel R_{I4} \parallel R_L$. Then, the currents at node V_y may be summed to find

$$g_{m,M1}V_x + \frac{V_y}{R_e} + \frac{V_y}{r_{\pi,Q2}+R_a} + \frac{V_y}{r_{o,Q2}} - \frac{V_z}{r_{o,Q2}} + \frac{\beta_{Q2}V_y}{r_{\pi,Q2}+R_a} = 0 \tag{37}$$

(37) can be simplified by using $A_{y\to z}$ from (34) to eliminate the V_z term. Then rearranging, the voltage gain is found to be

$$\frac{V_y}{V_x} = \frac{-g_{m,M1}}{\frac{\beta_{Q2}+1}{r_{\pi,Q2}+R_a} + \frac{1}{r_{o,Q2}} + \frac{1}{R_e} - \frac{1}{r_{o,Q2}A_{y\to z}}}. \tag{38}$$

To make (38) more tractable, a few assumptions can be made. First, this buffer is designed to drive low impedances. So, $R_L \ll r_{ds,M1}$ and $R_L \ll R_{I4}$, which makes $R_e \approx R_L$. Also, $\frac{1}{r_{o,Q2}A_{y\to z}} \ll \frac{1}{R_L}$ Thus, (38) simplifies to

$$\frac{V_y}{V_x} = \frac{-g_{m,M1}}{\frac{\beta_{Q2}+1}{r_{\pi,Q2}+R_a} + \frac{1}{R_L}} = -g_{m,M1}\left(\frac{r_{\pi,Q2}+R_a}{\beta_{Q2}+1} \parallel R_L\right). \tag{39}$$

Applying one final sanity check to (39), it is noted that it simplifies to the current gain of $M1$ multiplied by the resistance at the drain of $M1$ ($\approx \frac{1}{g_{m,Q2}} \parallel R_L$).

Finally, the loop gain can be determined by combining (36) and (39) to find

$$T = \left(\frac{V_z}{V_y}\right)\left(\frac{V_y}{V_x}\right) = -g_{m,M1}\left(\frac{\beta_{Q2}}{r_{\pi,Q2}+R_a}\right)(R_{I2} \parallel r_{o,Q2})\left(\frac{r_{\pi,Q2}+R_a}{\beta_{Q2}+1} \parallel R_L\right). \tag{40}$$

Having now found the loop gain, feedback theory in [9] leads to a closed-loop resistance looking into the base of $Q2$ of

$$R_c' = (R_c)(1-T) = R_c\left[1 + g_{m,M1}\left(\frac{\beta_{Q2}}{r_{\pi,Q2}+R_a}\right)(R_{I2} \parallel r_{o,Q2})\left(\frac{r_{\pi,Q2}+R_a}{\beta_{Q2}+1} \parallel R_L\right)\right]. \tag{41}$$

where R_c is taken from (32). So, the input impedance of the super-follower circuit is determined to be

$$R_{IN} = R_{I3} \parallel \left(\frac{1}{g_{m,Q1}} + R_{I1} \parallel R_c'\right). \tag{42}$$

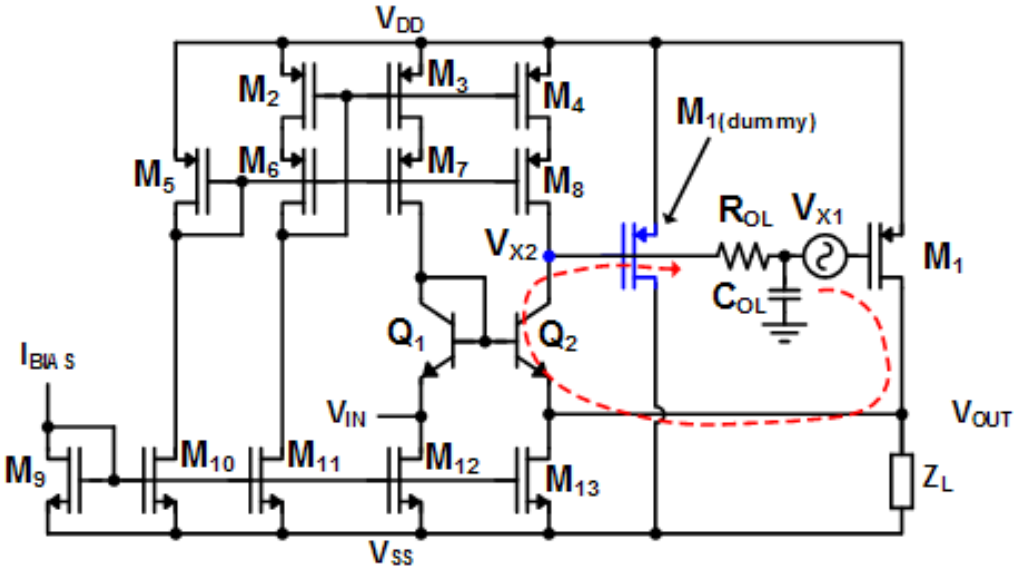

Figure 47: Super-follower circuit simulation for calculating loop-gain.

To simplify (42), assume that $R_c' \gg R_{I1}$, which leads to an input resistance of

$$R_{IN} \approx R_{I3} \parallel \left(\frac{1}{g_{m,Q1}} + R_{I1} \right). \tag{43}$$

At the output, the closed-loop resistance is determined to be

$$R_{OUT} = \frac{R_b \parallel R_{I4} \parallel r_{ds,M1} \parallel R_L}{1 - T}, \tag{44}$$

which may be simplified by assuming that both $r_{ds,M1}$ & $R_{I4} \gg R_L$ & R_B. This yields

$$R_{OUT} \approx \frac{R_L \parallel R_b}{1 + g_{m,M1} \left(\frac{\beta_{Q2}}{r_{\pi,Q2}+R_a} \right) (R_{I2} \parallel r_{o,Q2}) \left(\frac{r_{\pi,Q2}+R_a}{\beta_{Q2}+1} \parallel R_L \right)}. \tag{45}$$

4.5 Circuit AC Response and Simulation

Because the super-follower circuit has negative feedback, it is important to maintain adequate phase margin in the feedback loop. To stabilize feedback response, the circuit was simulated with the feedback loop open-circuited for AC response while maintaining DC bias as seen in Figure 47. R_{OL} effectively breaks the circuit for AC response simulations while C_{OL} AC grounds one side of the series voltage test

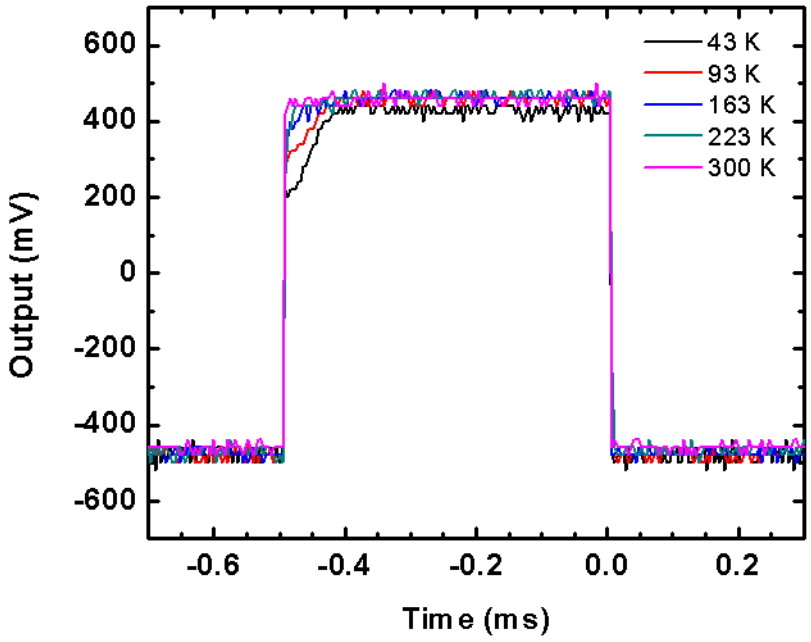

Figure 48: Output buffer response to a 1 V_{p-p} square wave input across temperature.

source, V_{X1}, to ground. For effective simulation in the bandwidth of interest, R_{OL} was chosen to be 1 GΩ and C_{OL} was chosen to be 1 F. A dummy load was applied to accurately reflect the loop self-compensation effect of pFET $M1$. The loop-gain response, V_{X2}/V_{X1} was measured, and the size of $M1$ was changed to provide adequate compensation for expected loads (simulated with $R_L = 50\ \Omega$ and $C_L = 100$ pF).

4.6 Buffer Testing

The buffer was tested in the closed-cycle cryostat test set up (refer to Section 2.6 for more details). The testing oscilloscope provided a 50 Ω load but had to be DC coupled for adequate measurement bandwidth at the low-frequency range. Thus, AVDD was set at 1.65 V while AVSS was set to -1.65 V to enable the scope to be DC coupled. The function generator was also DC coupled and applied a square-wave signal centered at ground. Results from a 1 V_{p-p}, 1 kHz square-wave input can be seen in Figure 48. Note that the rising edge of the buffer has curving features that

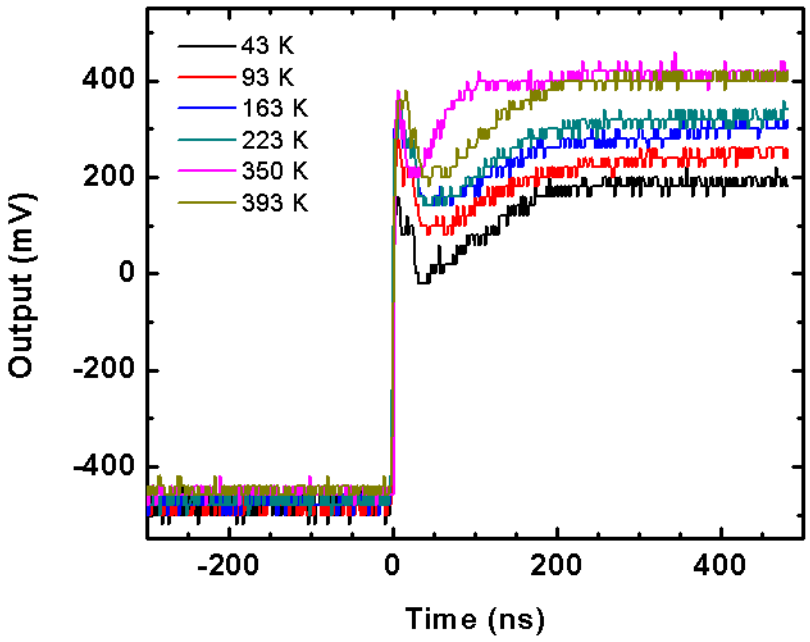

Figure 49: Buffer rising edge response to a 1 V_{p-p} square-wave input on a ns scale.

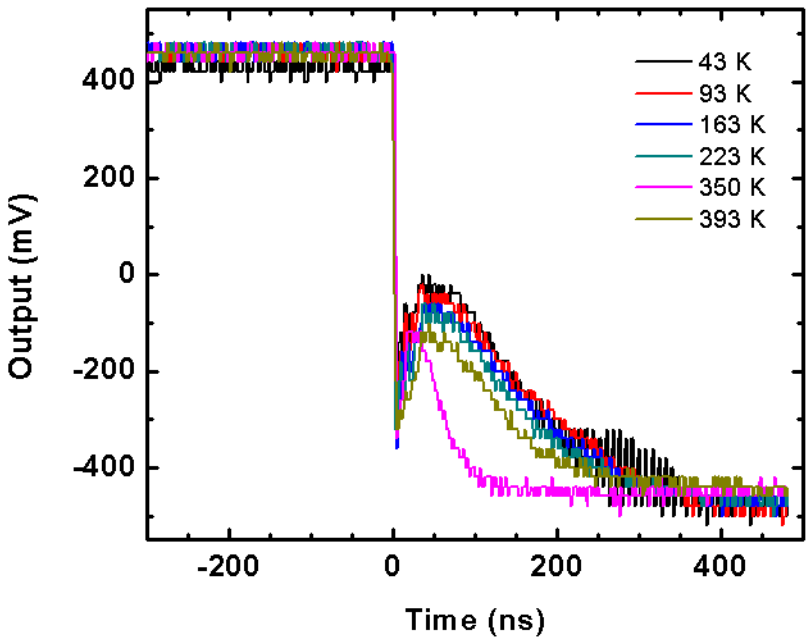

Figure 50: Buffer falling edge response to a 1 V_{p-p} square-wave input on a ns scale.

are accentuated with decreasing temperature. The nature of this effect is unknown, and is not predicted by simulation. The cryostat used for this testing is known to have limited bandwidth ($\approx$ 50 MHz), which may account for the effect seen. Further investigation will be necessary to pin-point the cause of this anomaly. The rising and falling edges of the buffer were measured on a nano-second scale and are shown in Figure 49 & 50 respectively. Simulations showed a pole-zero doublet type response as explained in [13], however, the degree of the response is much more pronounced in measurement. Again, this effect may be related to the limited bandwidth of the cryostat.

4.7 Summary

A high input-resistance, low output-resistance buffer was analyzed, designed, taped-out, and measured. The buffer shows promise as interface between an opamp or other analog circuit and a 50 Ω oscilloscope load typical of radiation test sites. This design may be used to enable future radiation testing of sensitive analog components.

CHAPTER V

CONCLUSION

This work has shown three different designs for interfacing on-die circuits with off-chip loads and communications buses: an RS-485 transceiver, a charge amplification channel, and a output buffer for 50 Ω loads. These circuits have been designed to be operable at temperatures ranging from -180°C to +120°C while maintaining tolerance to total ionizing dose of at least 100 krad and tolerance to single-event latch-up. These accomplishments have been enabled by the advantageous properties of the SiGe HBT as leveraged within a SiGe BiCMOS technology. Namely, the HBT has built-in tolerance to TID beyond 1 Mrad, and it's key performance parameters improve at cryogenic temperatures (β, g_m, f_T, & f_{max}).

Topics for future research include re-layout of the transmitter to compact its space requirements. Also, the transmitter needs to be laid-out with SEL tolerance in mind. The charge amplification channel has known issues with DC offset, which may be mitigated by using auto-zeroing opamps instead of purely analog topologies. Finally, these circuits' tolerance to single-event upset needs to be evaluated in the context of the space electronics application.

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